INTERNATIONAL ISLAMIC UNIVERSITY MALAYSIA
END OF SEMESTER EXAMINATION
SEMESTER I, 2011/2012 SESSION
KULLIYYAH OF ENGINEERING

Programme : ENGINEERING
Level of Study : UG 2

Time : 2:30 pm-5:30 pm
Date : 08/01/2012
Duration : 3 Hrs

Course Code : ECE 2133
Section(s) : 1

Course Title : **Electronic Circuits**

This Question Paper consists of **Six (6)** Printed Pages (Including cover and a blank page) with **Five (5)** Questions.

INSTRUCTION(S) TO CANDIDATES

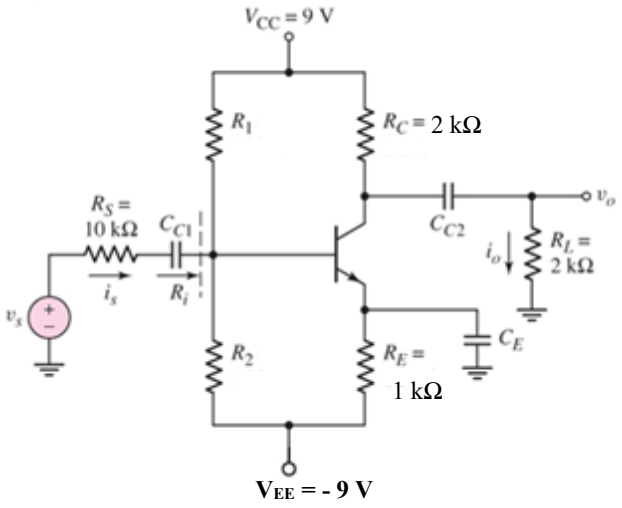
DO NOT OPEN UNTIL YOU ARE ASKED TO DO SO

- A total mark of this examination is **100**.
- This examination is worth **50%** of the total assessment.
- Answer **ALL FIVE (5)** questions.

Any form of cheating or attempt to cheat is a serious offence which may lead to dismissal.

Q.1 [20 marks]

(a) For the transistor parameters for the circuit is shown in **Fig. 1(a)** are β=100 and V_A=100. (**i**) Design the circuit such that it is biased stable and the V_{CEQ}= 1.0 V and V_{BE} =0.7 V. (**ii**) Find the small-signal hybrid-π parameters r_π, g_m and r_o and draw the small signal equivalent circuit for the midband frequency range. **(10 marks)**



$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

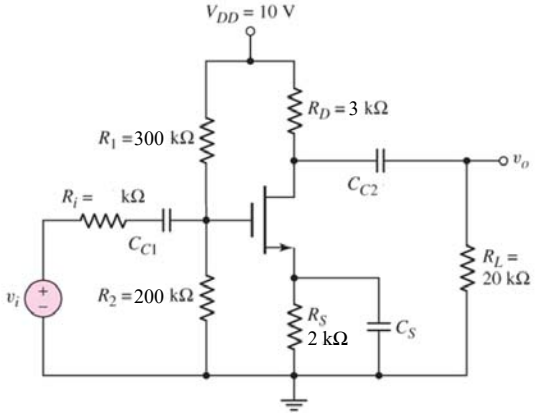
$$g_m r_\pi = \beta$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

Fig. 1(a)

(b) The FET circuit is shown in **Fig. 1(b)**, the transistor parameters are: K_n = 1 mA/V^2, V_{TN}=2V and λ = 0.01 V^{-1}. Find (**i**) the quiescent current I_{DQ}. (**ii**) Find the small-signal hybrid-π parameters g_m and r_o and draw the small signal equivalent circuit for the midband frequency range. All capacitors are 10 μF. **(10 marks)**



$$g_m = \sqrt{2K_n I_{DQ}}$$

$$r_o = \frac{1}{\lambda I_{DQ}}$$

Fig. 1(b)

Q.2 [20 marks]

(a) The common emitter transistor amplifier is shown in **Fig. 2(a)** and the transistor has small signal hybrid-π parameters, r_π = 4k**Ω**, g_m= 20mA/V and $r_o = \infty$. Find (**i**) the midband frequency voltage gain, $A_v = v_o/v_s$ and (**ii**) the input resistance R_i of the amplifier. **(10 marks)**

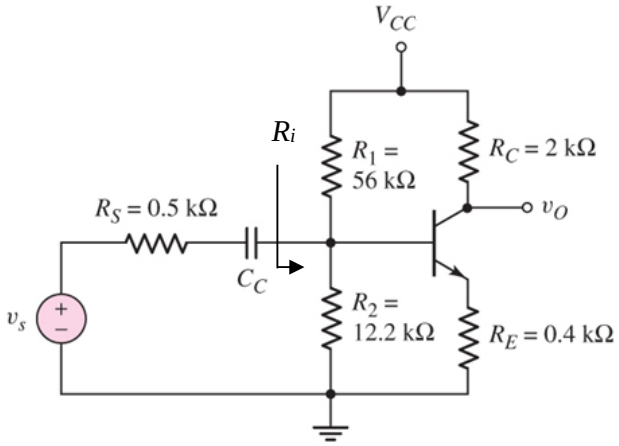


Fig. 2(a)

(b) The Darlington pair transistor is shown in **Fig. 2(b)**. Prove that the current of the Darlington pair amplifier is given by $A_i = \beta_1\beta_2$. [Symbols have their usual meanings] **(6 marks)**

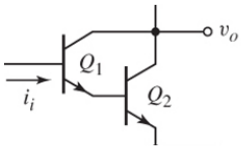


Fig. 2(b)

(c) Draw the Bode plot (magnitude and phase) of the following transfer functions. **(4 marks)**

(i) $H(s) = \dfrac{10}{(s+1000)}$ (ii) $H(s) = \dfrac{10000s}{(s+100)}$

Q.3 [20 marks]

(a) The common collector transistor amplifier is shown in **Fig. 3(a)** and the transistor has small signal hybrid-π parameters, $r_\pi = 4\ k\Omega$, $g_m = 20$ mA/V and $r_o = 100\ k\Omega$. The value of coupling capacitance is infinity. Find:

(i) the voltage gain, $A_v = v_o/v_s$ of the amplifier. **(2 marks)**
(ii) the current gain, $A_i = i_o/i_s$ the amplifier. **(3 marks)**
(iii) the input resistance, R_{is} of the amplifier. **(2 marks)**
(iv) the output resistance, R_o of the amplifier. **(3 marks)**

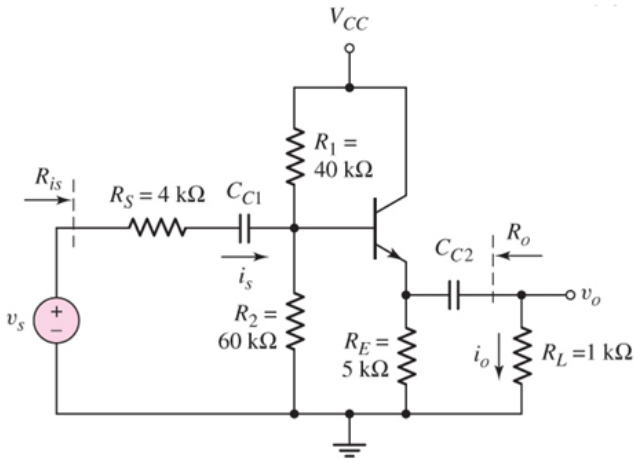


Fig. 3(a)

(b) Draw the typical frequency response of an amplifier and discuss the behavior of the response. **(3 marks)**

(c) Determine the lower 3 dB frequency (f_L) of the common emitter transistor with DC blocking capacitor as shown in **Fig. 3(c)**. The transistor parameters are: $V_{BE} = 0.7$ (on), $\beta = 120$, and $V_A = \infty$. [Other information can be found in this question] **(7 marks)**

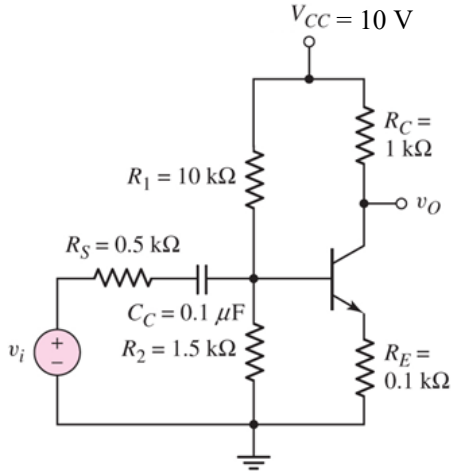


Fig 3(c)

Q.4 [20 marks]

(a) Determine the Miller capacitance and the upper 3 dB frequency (f_H) with and without Miller capacitance of the common emitter circuit shown in **Fig. 4(a).** The transistor parameters are: $r_\pi = 4\ k\Omega$, $g_m = 40$ mA/V and $r_o = \infty$, $C_\pi = 35$ pF, and $C_\mu = 4$ pF.

(10 marks)

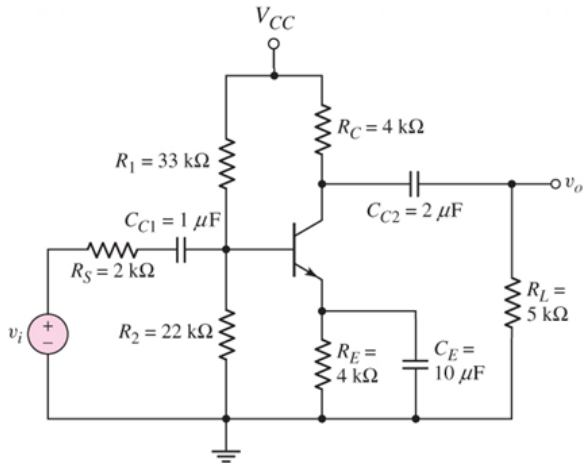


Fig. 4(a)

(b) Design a Wildlar current source as shown in **Fig. 4(b)** such that $I_{REF} = 1.5$mA and $I_o = 15\mu$A. Assume that $V^+ = +5$ V, $V^- = -5$ V, and $V_{BE1} = 0.7$ V. [Collector current is approximately given by $I_C = I_s e^{V_{BE}/V_T}$, where I_s is the reverse saturation current and V_T is the thermal voltage, $V_T = 26$ mV] **(10 marks)**

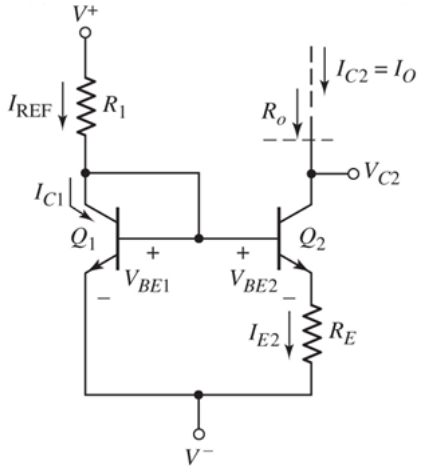


Fig. 4(b)

Q.5 [20 marks]

(a) Design a MOSFET current source as shown in **Fig. 5(a)** such that I_{REF} = 0.5mA and I_o= 0.1mA. The bias voltage V^+ = +5 V and V^- = -5 V. The transistors are available with parameters $k_n' = 40\mu A/V^2$, V_{TN} = 1 V and λ = 0. **(7 marks)**

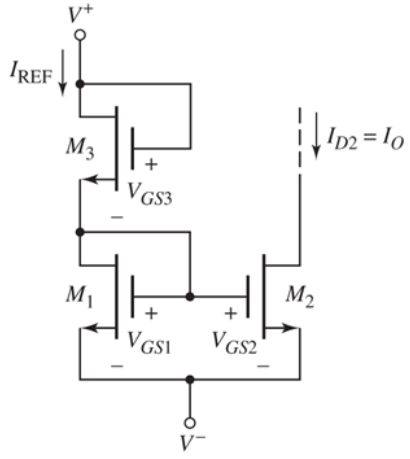


Fig. 5(a)

(b) What is a feedback system? Write down the advantages and disadvantages of a negative feedback amplifier. **(3 marks)**

(c) Draw the block diagram of a basic feedback amplifier and derive the closed-loop transfer function as $A_f = \dfrac{A}{1+\beta A}$. [The symbols have their usual meanings] **(4 marks)**

(d) The series-shunt feedback topology is shown in **Fig. 5(d)**. Draw the equivalent circuit configuration of an ideal series-shunt feedback amplifier. Derive the closed-loop voltage gain, A_f, input resistance with feedback, R_{if} and output resistance with feedback, R_{of}. **(6 marks)**

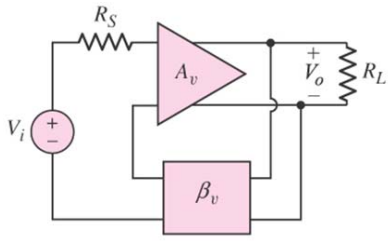


Fig. 5(d)