# OrCAD Flow Tutorial

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# Contents

# Introduction to the tutorial

# 1

This chapter consists of the following sections:



## Objective of the tutorial

To enable users to evaluate the power of the OrCAD PCB tools used in the Windows-based PCB design process. You can use this tutorial to perform all the steps in the PCB design process. The tutorial focuses on the sequence of steps to be performed in the PCB design cycle for an electronic design, starting with capturing the electronic circuit, simulating the design with PSpice, through the PCB layout stages, and finishing with the processing of the manufacturing output and maintaining the design through ECO cycles.

Tasks covered in this tutorial may not cover all the features of a tool. In this tutorial, the emphasis is on the steps that you will need to perform in each OrCAD tool so that your design works smoothly through the flow.

The tutorial design example used in this tutorial works within the limits of the demo version of tools available in the OrCAD 10.0 demo CD.

### Audience

This tutorial is useful for designers who want to use OrCAD tools for the complete PCB design flow or for analog simulation flow.

You can also benefit from the tutorial if you are a first-time user of OrCAD Capture, PSpice, OrCAD Layout, or SPECCTRA.

## Using the tutorial

To run through the complete tutorial, you need the design example and following tools:

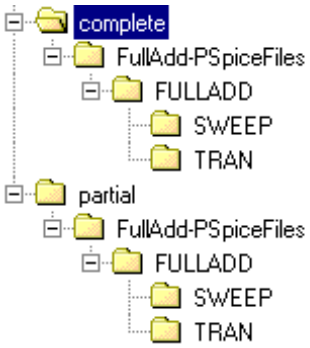
- OrCAD Capture
- PSpice A/D
- OrCAD Layout
- Spectra

All these tools are available in the Unison Ultra suite.

**Note:** This tutorial does not cover the tasks included in Capture CIS.

## Installing design example

Unzip the *demotut.zip* file provided with this design. When you expand the design, the following directory structure will be created.




The *partial* directory contains files generated at the end of Chapter 2, "Creating a schematic design." Use the files in this directory only if you want to skip the design creation steps covered in Chapter 2 and directly move on to Chapter 3 or Chapter 4.

The *complete* directory contains all the files generated through all the chapters in this tutorial. You can use the files in the *complete* directory to verify your results.

## Terminology

| | |
|---|---|
| OrCAD Capture | OrCAD's schematic design tool |
| Capture (initial CAPS) | The terms OrCAD Capture and Capture have been used interchangeably in the tutorial. |
| PSpice | OrCAD's simulation tool, used for simulating both Analog and digital circuits. |

| | |
|---|---|
| OrCAD Layout | OrCAD tool used for PCB routing and floor-planning |
| Layout | The terms OrCAD Layout and Layout have been used interchangeably in the tutorial. |

## What's next

In the next chapter, *Creating a schematic*, you will use OrCAD Capture for creating a schematic design. You will learn to perform basic design tasks such as adding components from a library, adding wires, and getting your design ready for simulation.

## Recommended reading

For more information about design suite configurations provided by OrCAD for affordable PCB design solutions, see the *OrCAD® Unison Suites Flow Guide*. For information about individual tools, see the respective User Guide.

# Creating a schematic design

# 2

This chapter consists of the following sections:



## Objective

To create a schematic design in OrCAD Capture. In this chapter, you will be introduced to basic design steps, such as placing a part, connecting parts using wires, adding ports, generating parts, and so on.

The steps for preparing your design for simulation using PSpice and for taking your design for placement and routing to OrCAD Layout are also covered in this chapter.

# Design example

In this chapter, you will create a full adder design in OrCAD Capture. The full adder design covered in this tutorial is a complex hierarchical design that has two hierarchical blocks referring to the same half adder design.

### Duration:

40 minutes

# Creating a design in Capture

## Guidelines

When creating a new circuit design in OrCAD Capture, it is recommended that you follow the guidelines listed below.

1. Avoid spaces in pathnames and filenames. This is necessary to get your design into downstream products, such as SPECCTRA.
2. Avoid using special characters for naming nets, nodes, projects, or libraries. While naming nets, use of illegal characters listed below might cause the netlister to fail.
   - ? (question mark)
   - @ (at symbol)
   - ~ (telda)
   - #(hash)
   - & (ampersand)
   - % (percent sign)
   - “ (quotation marks)
   - ! (exclamation mark)
   - ( )(parenthesis)
   - < (smaller than)

- = (equal)
- > (greater than)
- [ ](square parenthesis),
- * (asterisk)

## Creating a project

To create a new project, we will use Capture's Project Wizard. The Project Wizard provides you with the framework for creating any kind of project.

1. Launch Capture.
2. From the File menu, choose *New > Project*.
3. In the New Project dialog box, specify the project name as `FullAdd`.
4. To specify the project type, select *Analog or Mixed A/D*.

   **Note:** An Analog or Mixed A/D project can easily be simulated using PSpice. It also ensures that your design flows smoothly into OrCAD Layout for your board design.
5. Specify the location where you want the project files to be created and click OK.
6. In the Create PSpice Project dialog box, select the *Create a blank project* option button.

   **Note:** When you create a blank project, the project can be simulated in PSpice, but libraries are not configured by default. When you base your project on an existing project, the new project has same configured libraries.
7. Click OK to create the FullAdd project with the above specifications.

*Tip*

In case you already have a schematic design file (`.dsn`) that you want to simulate using PSpice, you need to create an Analog or Mixed A/D project using the *File > New > Project* command and then add your design to it.

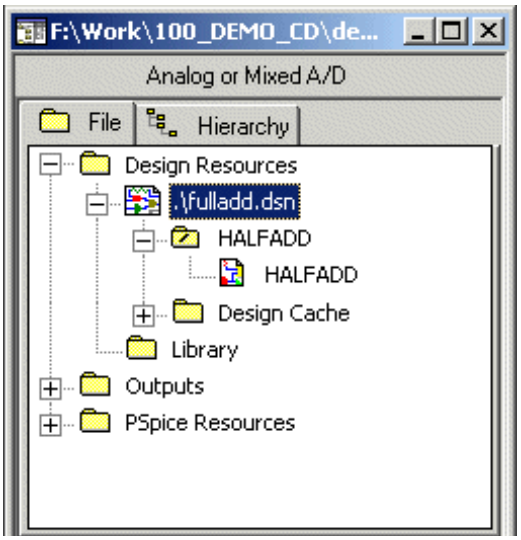
The FullAdd project is created. In the Project Manager window, a design file, `fulladd.dsn`, is created. Below the design file, a schematic folder with the name `SCHEMATIC1` is created. This folder has a schematic page named `PAGE1`.

## Renaming the schematic folder and the schematic page

You will now modify the design to change the name of both the schematic folder and the schematic page, to HALFADD.

1. In the Project Manager window, right-click on SCHEMATIC1.
2. From the pop-up menu, select *Rename*.
3. In the Rename Schematic dialog box, specify the name as `HALFADD`.
4. Similarly, right-click on PAGE1 and from the pop-up menu select *Rename*.
5. In the Rename Page dialog box, specify the page name as `HALFADD` and click OK.

After renaming of the schematic folder and the schematic page, the directory structure in the Project Manager window should be to similar to the figure below.




## Using a design template

Before you start with the design creation process in OrCAD Capture, you can specify the default characteristics of your project using the design template. A design template can be used to specify default fonts, page size, title block, grid references and so on. To set up a design template in OrCAD Capture, use the Design Template dialog box.

– To open the Design Template dialog box, from the Options drop-down menu choose Design Template.

To know more about setting up the design template, see *OrCAD Capture User's Guide*.

## Creating a flat design

In this section, we will create a simple flat half adder design with X and Y as inputs and SUM and CARRY as outputs.

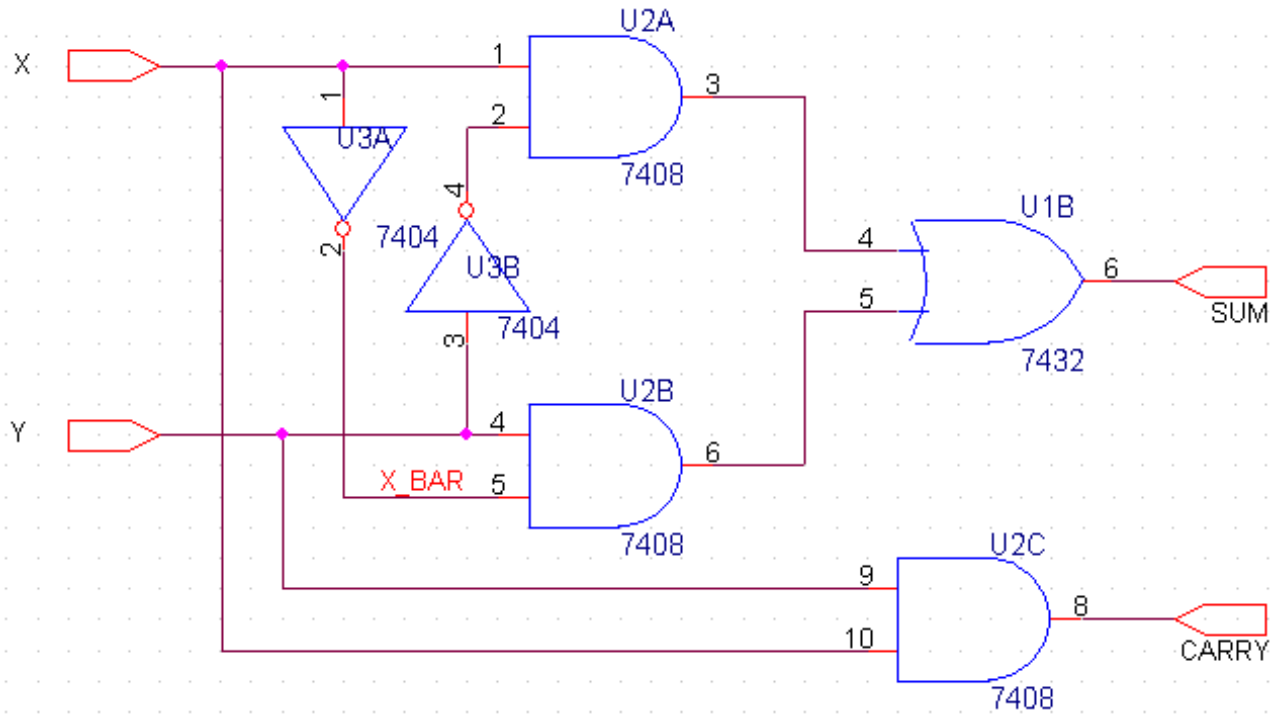



**Figure 2-1 Half adder design**

### Adding parts

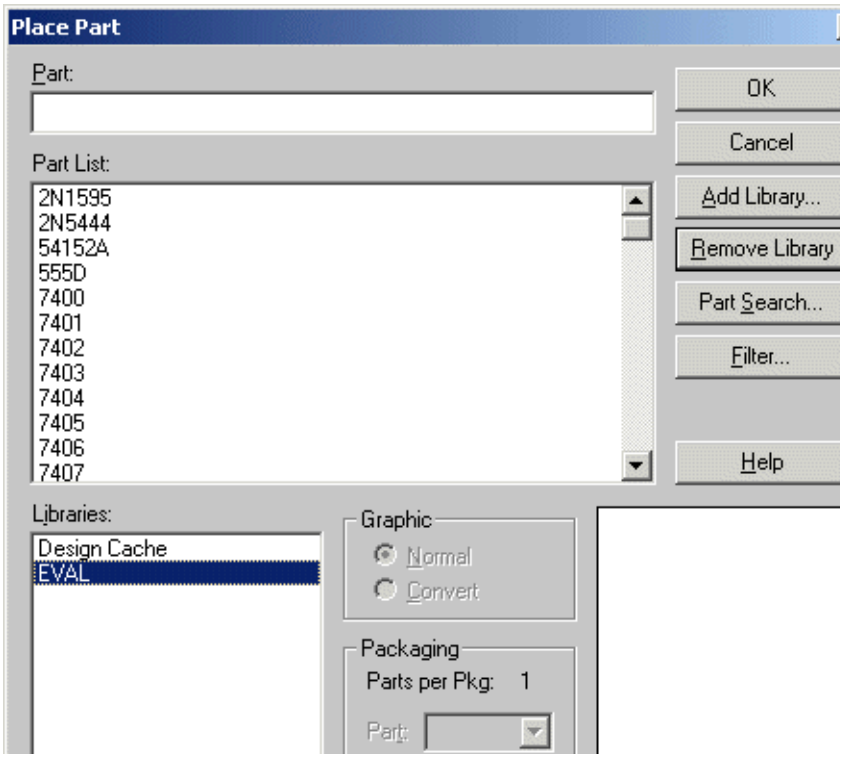
To add parts to your design:

1. From the Place menu in Capture, select Part.
2. In the Place Part dialog box, first select the library from which the part is to be added and then instantiate the part on the schematic page. While working with the demo version of Capture, you will add parts from EVAL.OLB.

   To add EVAL.OLB to the project, select the Add Library button.
3. Browse to *<install_dir>/tools/capture/library/pspice/eval.olb*.

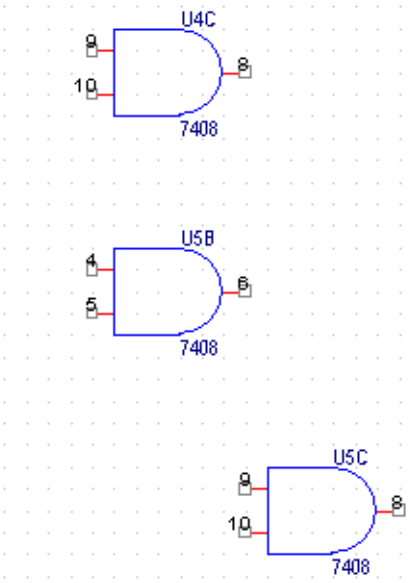
   Select EVAL.OLB and click Open.

The EVAL library appears in the *Libraries* list box.



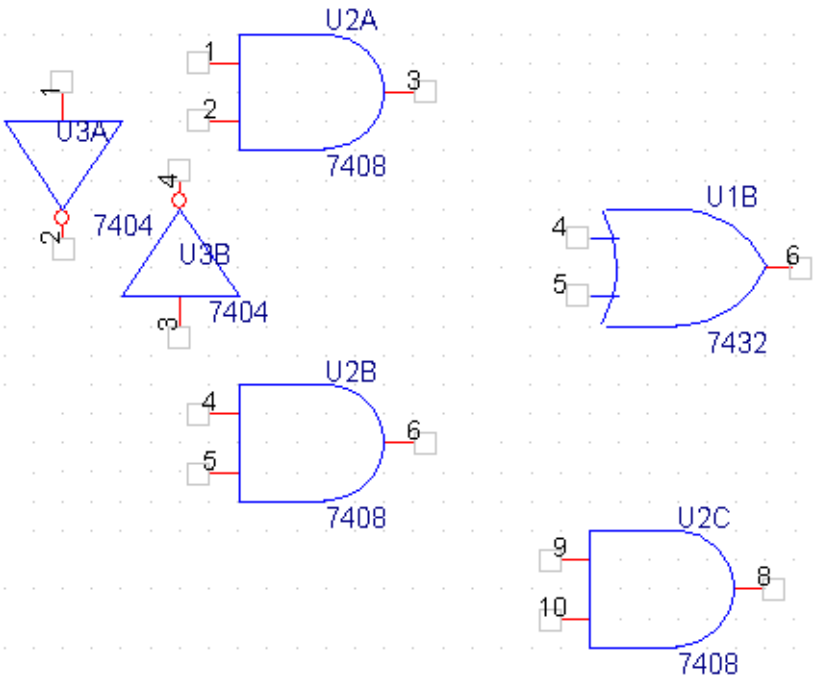

4 From the Part List, select `7408` and click OK.

5 Place three instances of the AND gate, `7408`, on the schematic page as shown in the figure below.



6 Right-click and select *End Mode*.

7 Place an OR gate (7432) and two NOT gates (7404) as shown in the figure below.




## Connecting parts

After placing the required parts on the schematic page, you need to connect the parts.

1 From the Place menu, choose Wire.

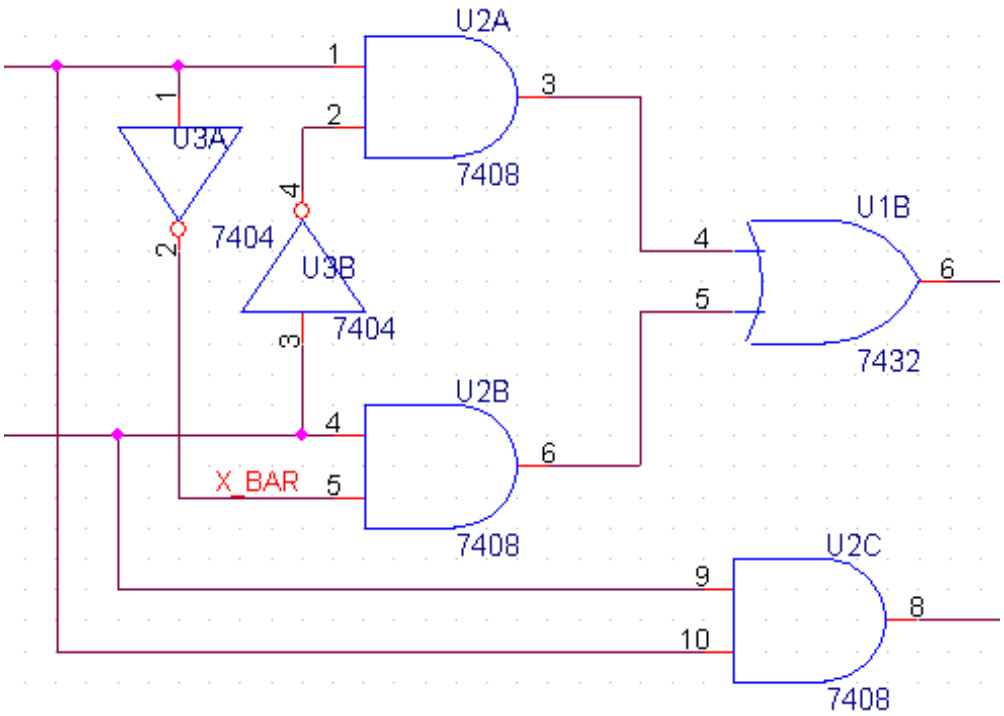
The pointer changes to a crosshair.

2 Draw the wire from the output of the AND gate, U2A, to the one of the inputs of the OR gate, U1B. To start drawing the wire, click the connection point of the output pin, `pin3`, on the AND gate.

3 Drag the cursor to input pin, `pin4`, of the OR gate (7432) and click on the pin to end the wire.

Clicking on any valid connection point ends a wire.

4 Similarly, add wires to the design until all parts are connected as shown in the figure below.




5 To stop wiring, right-click and select *End Wire*. The pointer changes to the default arrow.

## Adding ports

To add input and output ports to the design, complete the following sequence of steps:

1 From the *Place* menu in Capture, select *Hierarchical Port*.

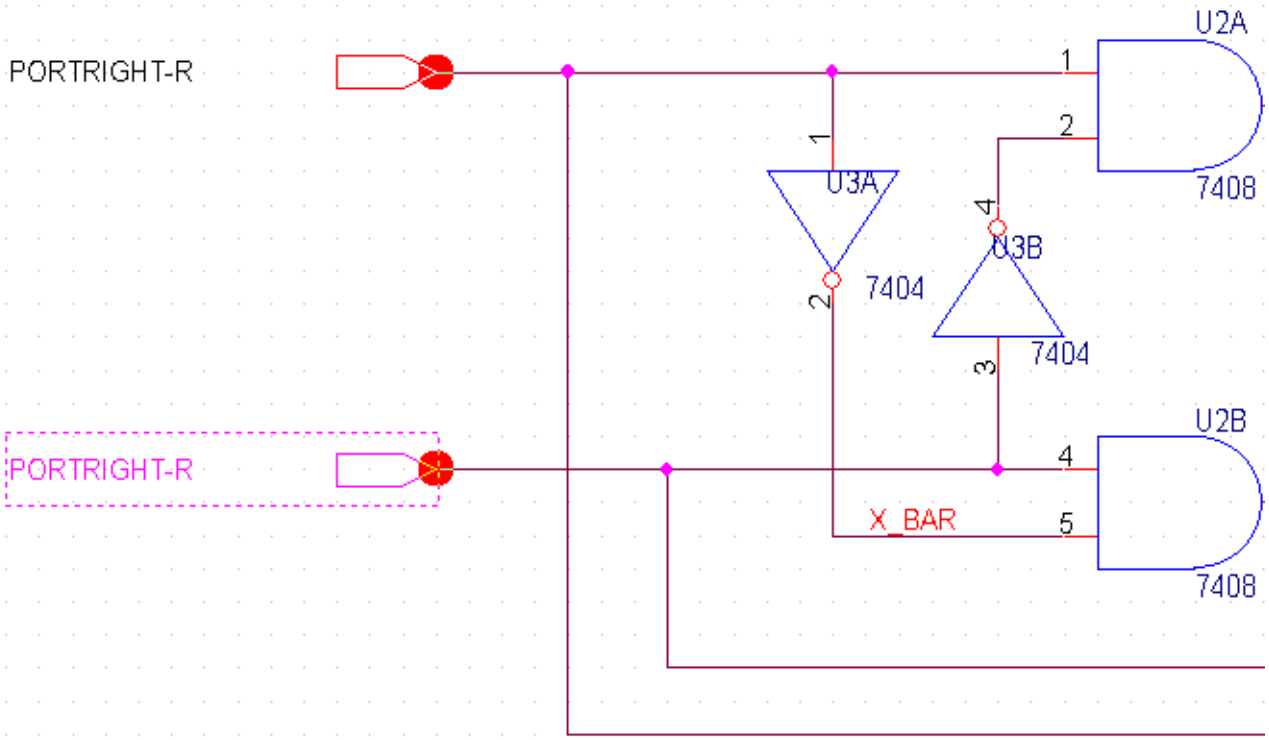
The Place Hierarchical Port dialog box appears.

**Note:** Alternatively, you can select the Place port button from the Tool Palette.

2 From the Libraries list box, select CAPSYM.

3 First add input ports. From the Symbols list, select `PORTRIGHT-R` and click OK.

4 Place two instances of the port as shown in the figure below




5 Right-click and select *End Mode*.

6 To rename the ports to indicate input signals X and Y, double-click the port name.

7 In the Display Properties dialog box, change the value of the Name property to X and click OK.

**Note:** You can also use the Property Editor to edit the property values of a component. To know the details, see *OrCAD Capture User's Guide*.

8 Similarly, change the name of the second port to Y.

**Note:** The Place Part dialog box is not used for placing ports, because ports in CAPSYM.OLB are only symbols and not parts. Only parts are listed in the Place Part dialog box.

9 Add two output ports as shown in the figure below. To do this, select `PORTLEFT-L` from the CAPSYM library.

10 Rename the ports to SUM and CARRY, respectively.

11 Save the design.

The half adder design is ready. The next step is to create a full adder design that will use the half adder design.

## Creating a hierarchical design

In Capture, you can create hierarchical designs using one of the following methods:

- Bottom-up method
- Top-down method

Another method of creating a hierarchical design is to create parts or symbols for the designs at the lowest level, and save the symbols in a user-defined library. You can later add the user-defined library in your projects and use these symbols in the schematic. For example, you can create a part for the half adder design and then instead of hierarchical blocks, use this part in the schematic. To know more about this approach, see Generating parts for a schematic.

In this section, we will create the full adder hierarchical design. The half adder design created in the Creating a flat design section will be used as the lowest level design.

### Bottom-up method

When you create a hierarchical design using the bottom-up methodology, you need to follow these steps.

- Create the lowest-level design.
- Create higher-level designs that instantiate the lower-level designs in the form of hierarchical blocks.

In this section, we will create a full adder design using bottom-up methodology. The steps involved are:

1 Creating a project in Capture. To view the steps, see Creating a project on page 13.

2 Creating the lowest-level design. In the full adder design example, the lowest-level design is the half adder design. To go through the steps for creating the half adder design, see Creating a flat design.

3 Creating the higher-level design. Create a schematic for the full adder design that uses the half adder design created in the previous step. To go through the steps, see Creating the full adder design.

### Creating the full adder design

1 In the Project Manager window, right-click on `fulladd.dsn` and select *New Schematic*.

2 In the New Schematic dialog box, specify the name of the new schematic folder as `FULLADD` and click OK.

In the Project Manager window, the FULLADD folder appears below `fulladd.dsn`.

3 Save the design.

4 To make the full adder circuit as the root design (high-level design), right-click on FULLADD and from the pop-up menu select *Make Root*.

The FULLADD folder moves up and a forward slash appears in the folder.

5 Right-click on FULLADD and select *New Page*.

6 In the New Page in schematic: FULLADD dialog box, specify the page name as *FULLADD* and click OK.

A new page, FULLADD, gets added below the schematic folder FULLADD.

7 Double-click the FULLADD page to open it for editing.

8 From the *Place* menu, choose *Hierarchical Block*.

9 In the Place Hierarchical Block dialog box, specify the reference as `HALFADD_A1`.

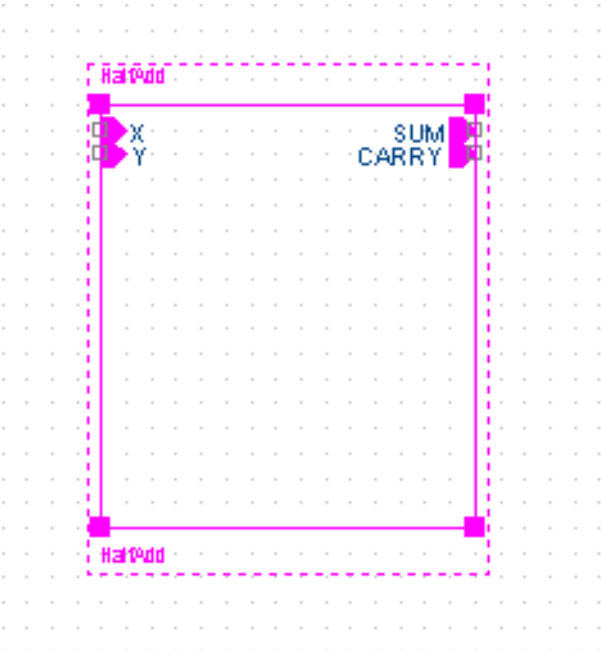
10 Specify the Implementation Type as Schematic View.

11 Specify the Implementation name as `HALFADD` and click OK.

The cursor changes to a crosshair.

12 Draw a rectangle on the schematic page.

A hierarchical block with input and output ports is drawn on the page.




13 If required, resize the block. Also, reposition the input and output ports on the block.

**Note:** To verify if the hierarchical block is correct, right-click on the block and select *Descend Hierarchy*. The half adder design you created earlier should appear.

14 Place another instance of the hierarchical block on the schematic page.

**a.** Select the hierarchical block.

**b.** From the *Edit* menu, choose *Copy*.

**c.** From the *Edit* menu, choose *Paste*.

**d.** Place the instance of the block at the desired location.

**Note:** Alternatively, you can use the <CTRL>+<C> and <CTRL>+<V> keys to copy-paste the block.

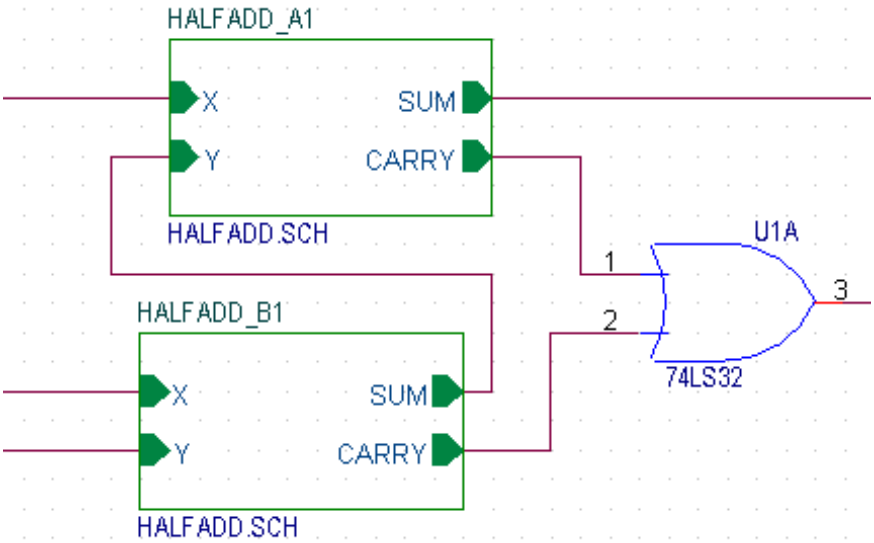
15 By default, the reference designator for the second hierarchical block is HALFADD_A2. Double-click on the reference designator, and change the reference value to `HALFADD_B1`.

16 Using the Place Part dialog box, add an OR gate (74LS32) to the schematic. (See Figure 2-2 on page 25.)

17 To connect the blocks, add wires to the circuit. From the *Place* menu, choose *Wire*.

18 Draw wires from all four ports on each of the hierarchical blocks.

19 Add wires until all the connections are made as shown in the figure below.




20 Add stimulus to the design. In the Place Part dialog box, use the Add Library button to add SOURCSTM.OLB to the design.

This library is located at *<install_dir>/tools/capture/library/pspice*.

21 From the Part List, select `DigStim1` and click OK.

The symbol gets attached to the cursor.

22 Place the symbol at three input ports: port X of the HALFADD_A1, port X and Y of HALFADD_B1.

23 Right-click on the schematic and select *End Mode*.

24 Specify the value of the Implementation property as Carry, X, and Y, respectively. See Figure 2-2 on page 25.

25 Select the Place Port button, to add an output port, CARRY_OUT, to the output of the OR gate. (See Figure 2-2 on page 25.)

26 From the list of libraries, select CAPSYM.

27 From the list of symbols, select PORTLEFT-L and click OK.

28 Place the output port as shown in the Figure 2-2 on page 25.

29 Double-click the port name and change the port to CARRY_OUT.

30 Save the design.

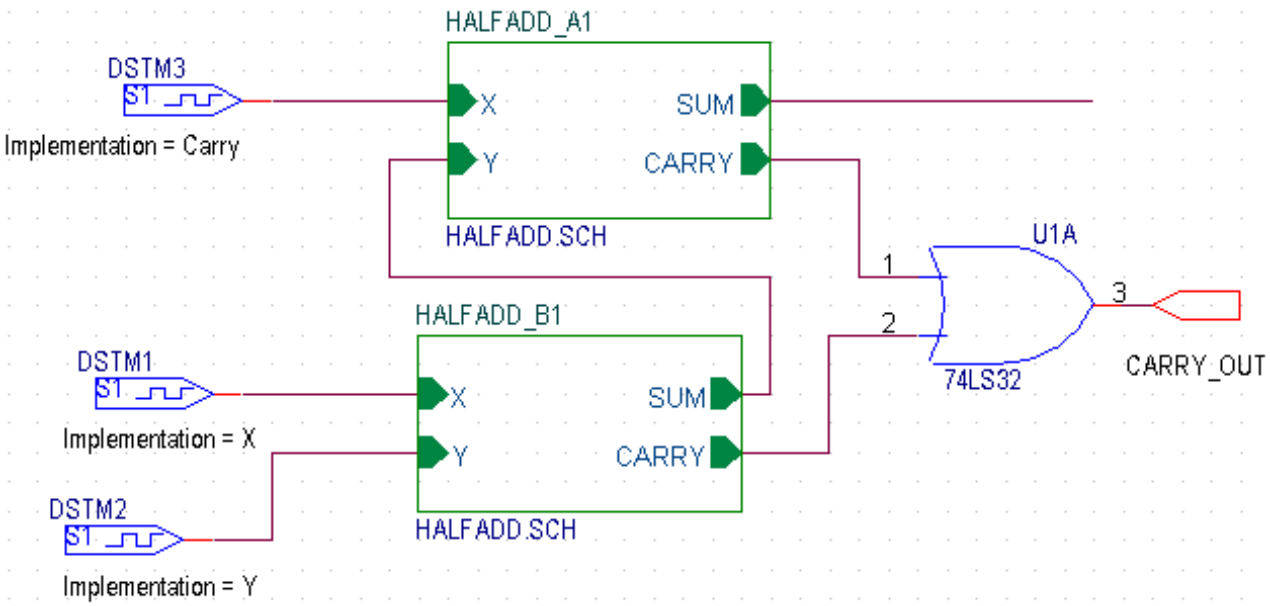



**Figure 2-2 The full adder circuit**

We have only added digital components to the design so far. We will now add a bipolar junction transistor to the SUM port of the HALFADD_A1 block.

1 Select the Place Part tool button.

2. In the Place Part dialog box, select the Add Library button.
3. Select `Analog.OLB`.
4. From the part list, add resistor R. Place this resistor on the schematic and connected one end of the resistor to the SUM port of HALFADD_A1. See Figure 2-3 on page 27.
5. From the EVAL.OLB, select `Q2N2222` and place it on the schematic. See Figure 2-3 on page 27.
6. Complete the circuit by adding a collector resistance, Collector Voltage, and ground. See Figure 2-3 on page 27.

### Adding Collector Voltage

**a.** To add the voltage, add the SOURCE.OLB library to the project.

**b.** From the Part List select VDC and click OK.

**c.** Place the voltage source on the schematic. See Figure 2-3 on page 27.

**d.** By default, the source is of 0 volts. Using the Property Editor, change it to a voltage source of 5V. To do this, double-click the voltage source.

**e.** In the Property Editor window, change the value of the DC parameter to 5.

**f.** Save and close the Property Editor window.

### Adding Ground

**a.** To add ground, select the Place ground 

button.

**b.** In the Place Ground dialog box, select the SOURCE library.

**c.** From the part list, select 0 and click OK.

**d.** Place the ground symbol on the schematic. See Figure 2-3 on page 27.

*Important*

You must use the 0 ground part from the SOURCE.OLB part library. You can use any other ground part only if you change its name to 0.

**7** Add a connector CON2 to the circuit. To do this, add a Capture library, CONNECTOR.OLB to the project.

CONNECTOR.OLB is located at *<install_dir>/tools/capture/library.*

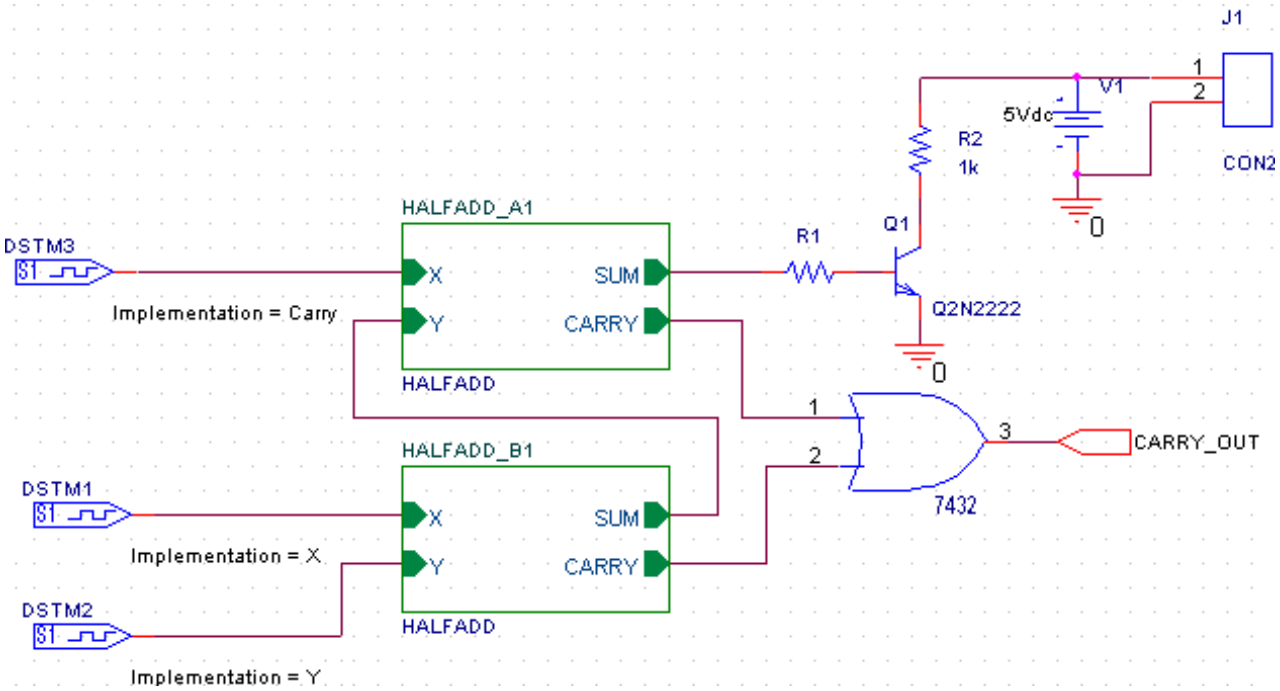



**Figure 2-3 Full adder circuit with output through a transistor**

You have successfully created the full adder hierarchical design using the bottom-up methodology. As the components used in this design are from the PSpice library, you can simulate this design using PSpice.

## Top-down method

When you create a hierarchical design using the top-down methodology, use the following sequence of steps:

- Create the top-level design using functional blocks, the inputs and outputs of which are known.
- Create a schematic design for the functional block used in the top-level design.

This section provides an overview of the steps to be followed for creating a full adder using top-down methodology.

1 Create a FullAdd project.
To view the steps, see Creating a project on page 13.

2 Create the top-level design, using the following steps:

**a.** From the *Place* menu, choose *Hierarchical Block*.

**Note:** Alternatively, you can select the Place hierarchical block button  from the Tool Palette.

**b.** In the Place Hierarchical Block dialog box, specify the reference as `HALFADD_A1`, Implementation Type as `Schematic View`, Implementation name as `HALFADD`, and click OK.

See Step 9 to Step 11 in the Bottom-up method section.

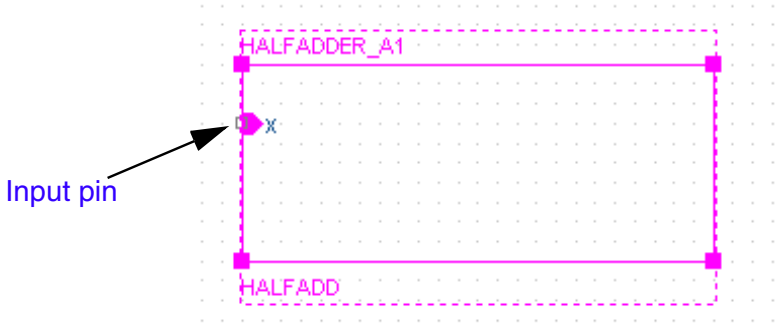
**c.** Draw the hierarchical block as required.

Note that unlike the hierarchical block drawn in the bottom-up methodology, the hierarchical block in the top-down methodology does not have port information attached to it.

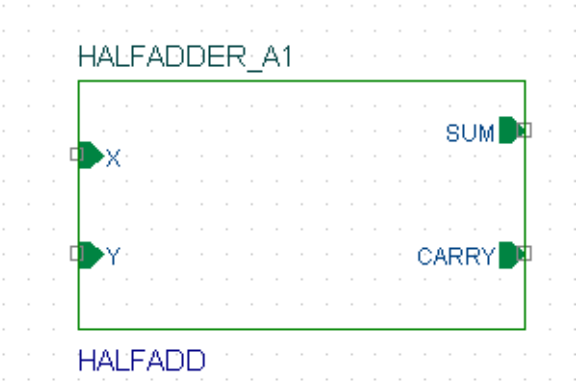
**d.** Select the hierarchical block and then from the *Place* menu, choose *Hierarchical Pins*.

**e.** In the Place Hierarchical Pin dialog box, specify the pin name as `X`, Type as `Input`, and Width as `Scalar` and click OK.

**f.** Place the pin as shown in the figure below.

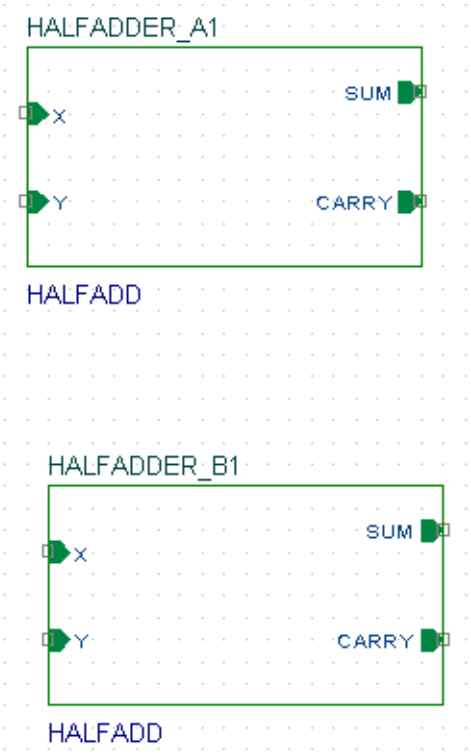



**g.** Similarly, add another input pin Y and two output pins, SUM and CARRY, as shown in the figure below.




**h.** Place another hierarchical block with the Implementation Type as HALFADD. The easiest way to do this is to copy the existing hierarchical block and paste it on the schematic page.

By default, the reference value of the second hierarchical block is HALFADD_A2. Change this value to HALFADD_B1.




**i.** Complete the full adder circuit by adding ports, wires, and stimuli. See The full adder circuit on page 25.

**j.** Save the design.

**3** Draw the lowest-level design using the steps listed below. For the full adder design example, the lowest-level design is a half adder circuit.

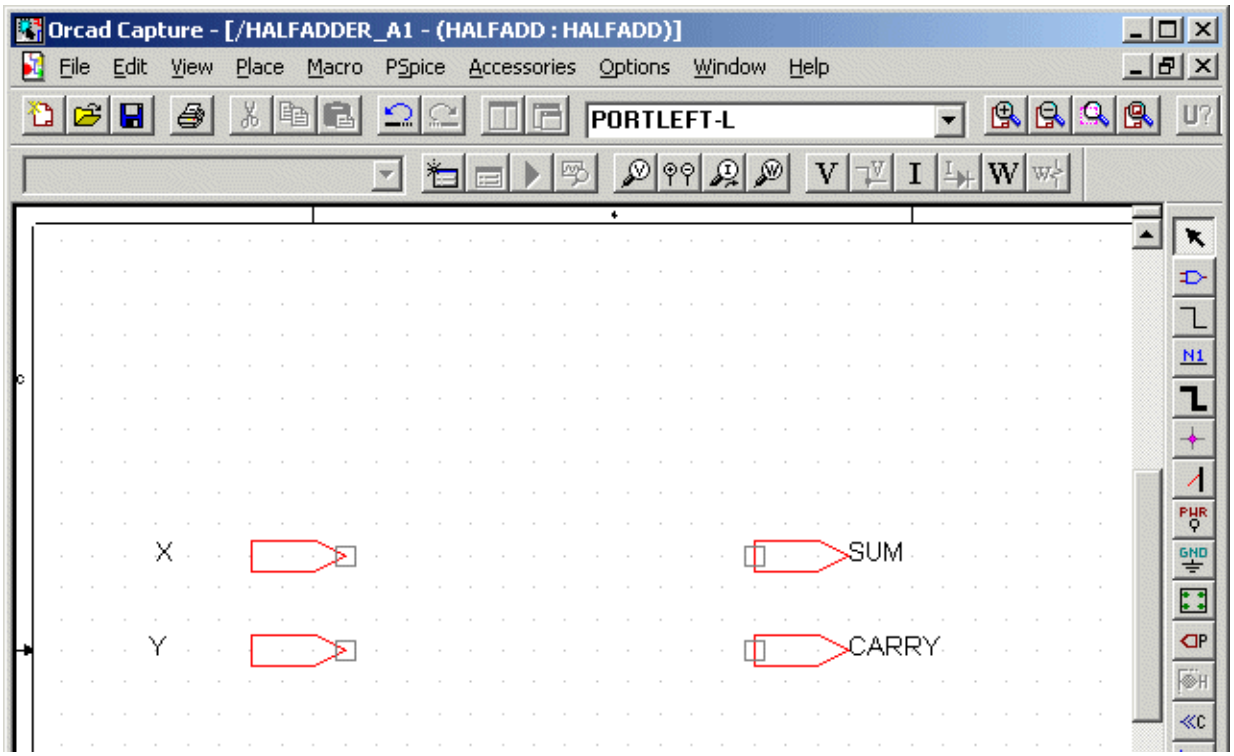
**a.** To draw the half adder design, right-click on any one of the HALFADD hierarchical block.

**b.** From the pop-up menu, select *Descend Hierarchy*.

**c.** The New Page in Schematic: 'HALFADD' dialog box appears.

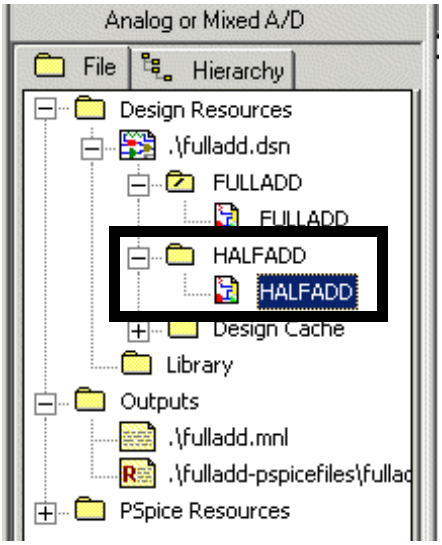
Specify the page name as `HALFADD` and click OK.

A new schematic pages appears with two input ports, X and Y, and two output ports, SUM and CARRY.




You can now draw the half adder circuit on this schematic page using the steps covered in the Creating a flat design on page 16. Also see Figure 2-1 on page 16.

In the Project Manager window, a new schematic folder HALFADD gets added below `fulladd.dsn`.




## Generating parts for a schematic

Instead of creating a hierarchical block for the half adder design, you can generate a part for the half adder design and then reuse the part in any design as and when required.

In this section of the tutorial, we will generate a part for the half adder circuit that you created in the Creating a flat design section of this chapter.

To generate a part from a circuit, complete the following steps.

1. In the Project Manager window, select the HALFADD folder.
2. From the *Tools* menu, choose *Generate Part*.
3. In the Generate Part dialog box, specify the location of the design file that contains the circuit for which the part is to be made.

   For this design example, specify the location of `fulladd.dsn`.
4. In the *Netlist/source file type* drop-down list box, specify the source type as `Capture Schematic Design`.

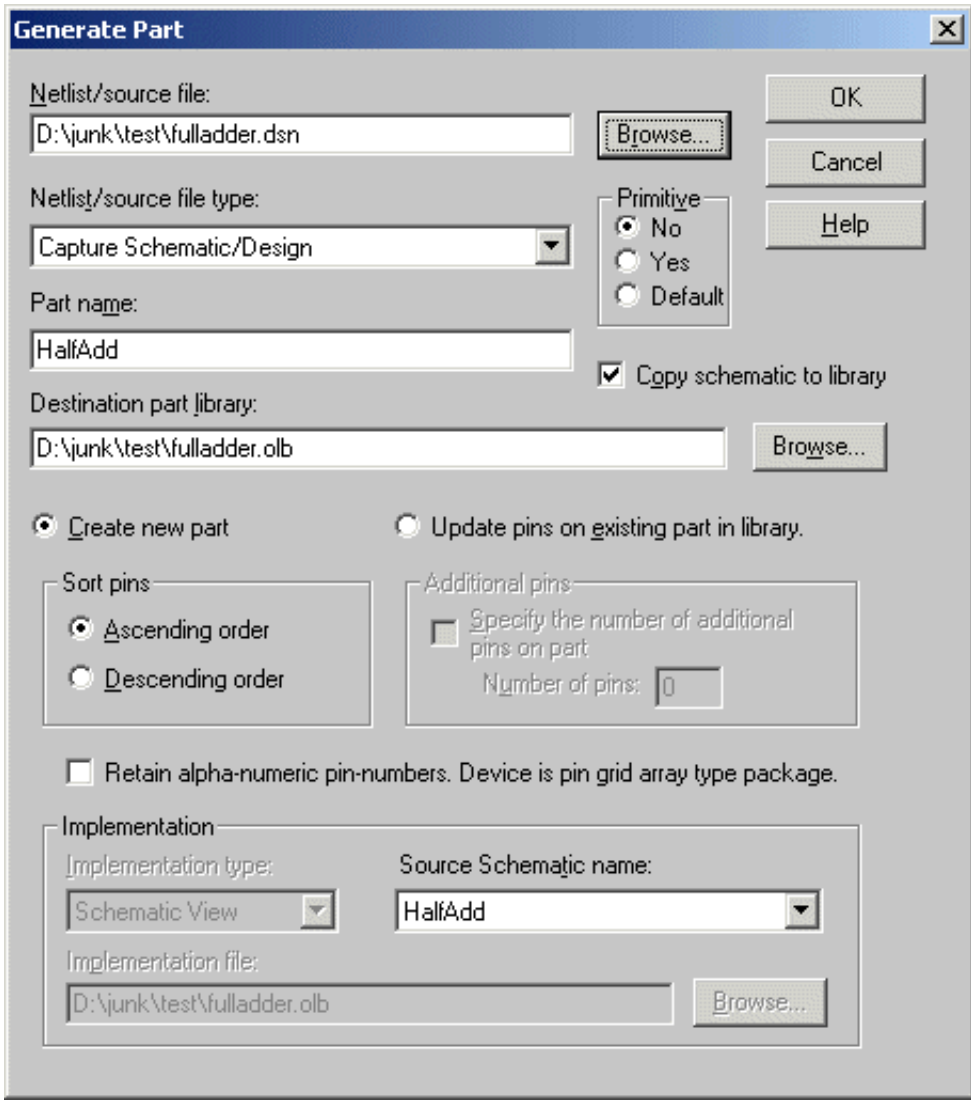
5 In the *Part Name* text box, specify the name of the part that is to be created, as `HALFADD`.

6 Specify the name and the location of the library that will contain this new part being created. For the current design example, specify the library name as `Fulladd.olb`.

7 If you want the source schematic to be saved along with the new part, select the *Copy schematic to library* check box. For this design, select the check box.

8 Ensure that the *Create new part* option is selected.

9 To specify the schematic folder that contains the design for which the part is to be made, select HALFADD from the Source Schematic name drop-down list box.




10 Click OK to generate the HalfAdd part.

A new library, `fulladd.olb`, is generated and is visible under the Outputs folder in the Project Manager window. The new library also gets added in the Place part dialog box. You can now use the Place part dialog box to add the half adder part in any design.

### Navigating through a hierarchical design

To navigate to the lower levels of the hierarchy, right-click a hierarchical block and choose *Descend Hierarchy*.

Similarly, to move up the hierarchy, right-click and select *Ascend Hierarchy*.

The *Ascend Hierarchy* and *Descend Hierarchy* menu options are also available in the *View* drop-down menu.

While working with hierarchical designs, you can make changes to the hierarchical blocks as well as to the designs at the lowest level.

To keep the various hierarchical levels updated with the changes, you can use the Synchronize options available in the View drop-down menu.

Select *Synchronize Up* when you have made changes in the lowest-level design and want these changes to be reflected higher up in the hierarchy.

Select *Synchronize Across* when you have made changes in a hierarchical block and want the changes to be reflected across all instances of the block.

Select *Synchronize Down* when you have made changes in a hierarchical block and want these changes to be reflected in the lowest-level design.

## Processing a design

After you have created your schematic design, you may need to process your design by adding information for tasks such as, simulation, synthesis, and board layout. This section covers some of the tasks that you can perform in OrCAD Capture while processing your design.

## Adding part references

To be able to take your schematic design to the Layout for packaging, you need to ensure that all the components in the design are uniquely identified with part references. In OrCAD Capture you can assign references either manually or by using the Annotate command.

In the full adder design, annotation is not required at this stage because by default, unique part references are attached to all the components. This is so because by default, Capture adds part reference to all the components placed on the schematic page. If required, you can disable this feature by following the steps listed below.

1. From the *Options* menu, choose *Preferences*.
2. In the Preferences dialog box, select the Miscellaneous tab.
3. In the Auto Reference section, clear the *Automatically reference placed parts* check box.
4. Click OK to save these settings.

In case the components in your design do not have unique part references attached to them, you must run the Annotate command.

To assign unique part references to the components in the FULLADD design using the Annotate command, complete the following steps:

1. In the Project Manager window, select the `fulladd.dsn` file.
2. From the *Tools* drop-down menu, choose *Annotate*.

   **Note:** Alternatively, you can click the Annotate  button on the toolbar.
3. In the Packaging tab of the Annotate dialog box, specify whether you want the complete design or only a part of the design to be updated. Select the *Update entire design* option button.
4. In the Actions section, select the *Incremental reference update* option button.

**Note:** To know about other available options, see the dialog box help.

5 The full adder design is a complex hierarchical design. So choose the *Update Occurrence* option button.

**Note:** When you select the Update Occurrence option, you may receive a warning message. Ignore this message because for all complex hierarchical designs, the occurrence mode is the preferred mode.

6 For the rest of the options, accept default values and click OK to save your settings.

The Undo Warning message box appears.

7 Click Yes.

A message box stating that the annotation will be done appears.

8 Click OK.

Your design is annotated and saved. You can view the value of updated cross reference designators on the schematic page.

*Caution*

If you select the Annotate command after generating the Layout netlist, you will receive an error message stating that annotating at this stage may cause the board to go out of sync with the schematic design. This may cause further backannotation problems.

## Creating a cross reference report

Using Capture, you can create cross reference reports for all the parts in your design. A cross reference report contains information, such as part name, part reference, and the library from which the part was selected.

To generate a cross reference report using Capture:

1 From the Tools menu choose Cross References.

Alternatively, you can choose the cross reference parts  button from the toolbar.

2 In the Cross Reference Parts dialog box, ensure that the *Cross reference entire design* option button is selected.

**Note:** If you want to generate the cross reference report for a particular schematic folder, select the schematic folder before opening the Cross Reference Parts dialog box, and then select the cross reference selection option button.

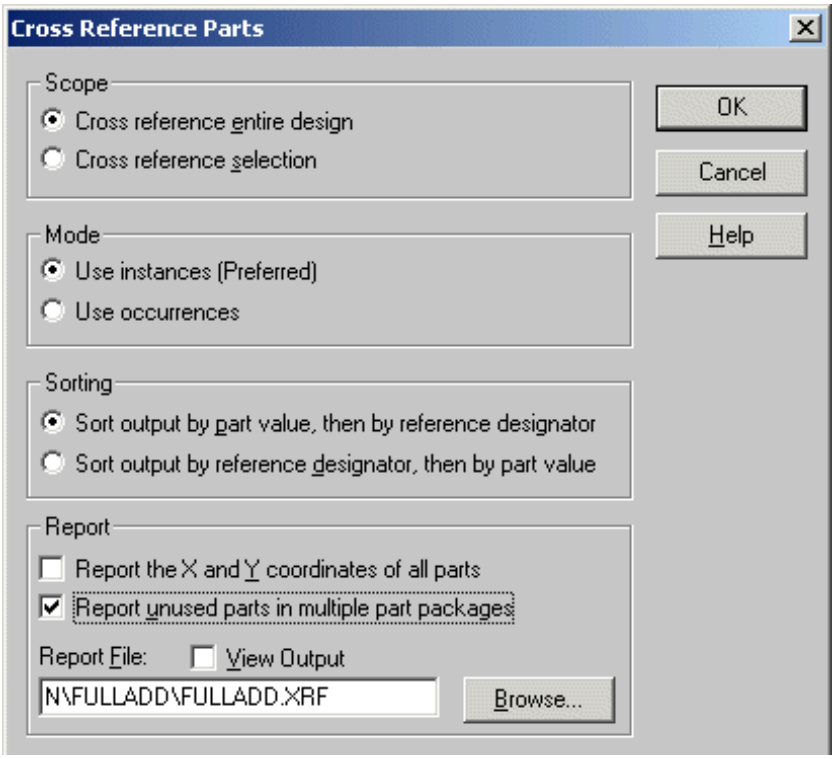
3 In the Mode section, select the *Use Occurrences* option button.

**Note:** Ignore the warning that is displayed when you select the Use Occurrences mode. For complex hierarchical designs, you must always use the occurrence mode.

4 Specify the report that you want to be generated.

5 In case you want the report to be displayed automatically, select the View Output check box.

6 Click OK to generate the report.




A sample output report is shown below.

File Edit Format Help

Revised: Wednesday, January 28, 2004
Revision:

Design Name: D:\FULLADDDESIGN\FULLADD.DSN

Cross Reference January 28,2004 12:02:24 Page1

| Item | Part | Reference | SchematicName | Sheet | Library |
|---|---|---|---|---|---|
| 1 | 1K | R1 | /FULLADD | 1 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE\LIBR |
| 2 | 1K | R2 | /FULLADD | 1 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE\LIBR |
| 3 | 7404 | U3A | HALFADD_A1/HALFADD | 2 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTI |
| 4 | 7404 | U3B | HALFADD_A1/HALFADD | 2 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTI |
| 5 | 7404 | U3C | HALFADD_B1/HALFADD | 3 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTI |
| 6 | 7404 | U3D | HALFADD_B1/HALFADD | 3 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTI |
| 7 | 7408 | U2A | HALFADD_A1/HALFADD | 2 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTI |
| 8 | 7408 | U2B | HALFADD_A1/HALFADD | 2 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTI |
| 9 | 7408 | U2C | HALFADD_A1/HALFADD | 2 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTI |
| 10 | 7408 | U2D | HALFADD_B1/HALFADD | 3 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTI |
| 11 | 7408 | U4A | HALFADD_B1/HALFADD | 3 | C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTI |

## Generating a bill of materials

After you have finalized your design, you can use Capture to generate a bill of materials (BOM). A bill of materials is a composite list of all the elements you need for your PCB design. Using Capture, you can generate a BOM report for electrical and as well as non-electrical parts, such as screws. A standard BOM report includes the item, quantity, part reference, and part value.

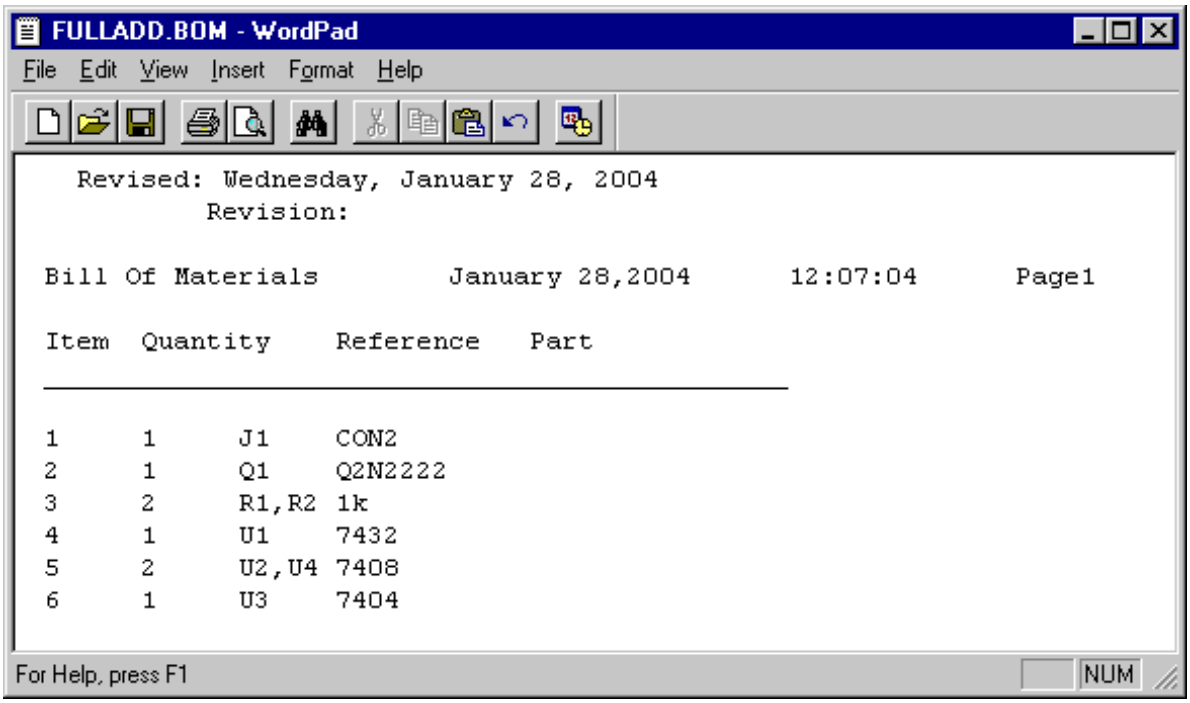
To generate a BOM report:

1. In the Project Manager window, select `fulladd.dsn`.
2. From the *Tools* menu, select *Bill of Materials*.
3. To generate a BOM report for the complete design, ensure that the Process entire design option button is selected.
4. For a complex hierarchical designs, the preferred mode is the occurrence mode. Therefore, select the *Use Occurrences* option button.

   **Note:** In case you receive a warning stating that it is not the preferred mode, ignore the warning.
5. Specify the name of the BOM report to be generated. For the current design, accept the default name, `FULLADD.BOM`.

   **Note:** By default, the report is named as *`designname.BOM`*.
6. Click OK.

The BOM report is generated. A sample report is shown below:




## Getting your design ready for simulation

To be able to simulate your design using PSpice, you must have the connectivity information and the simulation settings for the analysis type to be done on the circuit design.

The simulation setting information is provided by a simulation profile (`*.SIM`). This section covers the steps to be followed in Capture for creating a simulation profile.

**Note:** To know more details about getting your design ready for simulation using PSpice, see *Chapter 3, Preparing a design for simulation* of the *PSpice User's Guide*.

### Creating a simulation profile from scratch

To create a new simulation profile to be used for transient analysis, complete the following steps:

1. From the PSpice menu in Capture, choose New Simulation Profile.
2. In the New Simulation dialog box, specify the name of the new simulation profile as TRAN.
3. In the Inherit From text box, ensure that none is selected and click Create.

   The Simulation Setting dialog box appears with the Analysis tab selected.
4. In the Analysis type drop-down list box, Time Domain (Transient) is selected by default. Accept the default setting.
5. Specify the options required for running a transient analysis. In the Run to time text box, specify the time as 100u.
6. Click OK to save your modifications and to close the dialog box.

You can now run transient analysis on the circuit. Note that the Simulation Setting dialog box also provides you with the options for running advanced analysis, such as Monte Carlo (Worst Case) analysis, Parametric analysis and Temperature analysis. You may choose to run these as and when required.

**Note:** To know details about each option in the Simulation Settings dialog box, click the Help button in the dialog box.

## Creating a simulation profile from an existing profile

You can create a new simulation profile from an existing simulation profile. This section covers the steps for creating a new simulation profile, SWEEP, from an existing simulation profile, named TRAN.

1. From the *PSpice* menu, choose *New Simulation Profile*.
2. In the New Simulation dialog box, specify the profile name as `SWEEP`.

3 In the Inherit From drop-down list box, select FULLADD-TRAN.

4 Click the Create button.

The Simulation Settings dialog box appears with the general settings inherited from the existing simulation profile. You can now modify the settings as required and run PSpice to simulate your circuit.

## Adding Layout specific properties

To be able to take your design to OrCAD Layout for placement and routing, you need to add the footprint information for each of the components in your design.

By default, some footprint information is available with all the components from the PSpice-compatible libraries located at *<install_dir>/tools/capture/library/pspice*. However, these footprints are not valid. You need to change these values to valid footprint values. You can add footprint information either at the schematic design stage in OrCAD Capture or during the board design stage in OrCAD Layout. In this section, you will learn to add footprint information to the design components during the schematic design stage.

To add footprint information to the OR gate, 7432, in the FULLADD schematic page, complete the following steps.

1 Right-click on the OR gate and select *Edit Properties*.

The Property Editor window appears.

2 In the Filter by drop-down list box, select Orcad-Layout.

The columns in the spreadsheet display the Layout properties.

3 To change the value of the PCB Footprint property, click on the corresponding cell and type in the value as `SOG.050/14/WG.244/L.350`.

4 Press ENTER or click Apply.

**Note:** To assign PCB footprints to your schematic parts, select the Layout footprint names from OrCAD Layout

Footprint Libraries or from your custom footprint libraries.

5 Save the changes and close the Property Editor window.

Similarly, add PCB footprint information for all the components in the design. The component name and the corresponding footprint information to be added is listed in the table below.

| Component... | PCB Footprint... |
|---|---|
| AND gate (7408) | SOG.050/14/WG.244/L.350 |
| OR gate (7432) | SOG.050/14/WG.244/L.350 |
| NOT gate(7404) | SOG.050/14/WG.244/L.350 |
| Resistance | SM/R_0805 |
| Connector(CON2) | SIP/TML/L.200/2 |

Your design is now ready to be taken to OrCAD Layout for placement and routing.

## Design rules check

After you have completed your design, it is recommended that you run design rules check (DRC) to isolate any unwanted design errors that might be there in the design.

To run DRC on the full adder design, complete the following steps:

1 In the Project Manager window, select the design file, `fulladd.dsn`.

2 From the *Tools* menu, select *Design Rule Checks*.

**Note:** Alternatively, you can select the Design Rule Checks button  from the toolbar.

3 In the Design Rules Check dialog box, the Design Rules Check tab is selected by default. Specify your preferences.

By default, the *Check entire design* option button is selected. To run DRC on the complete design, accept the default selection.

4 Select the *Use Occurrences* option button.

**Note:** For complex hierarchical designs, the occurrence mode is the preferred mode. Therefore, ignore the warning that is displayed when you select the Use occurrences option button.

5 To run the DRC, select the *Check design rule* option button.

6 In the Report section, select appropriate check boxes to specify what all is required in the DRC report.

For the current design example, select the *Check unconnected nets* and *Report identical part references* check boxes.

7 Select the *View Output* check box.

When this check box is selected, the DRC report is opened automatically for viewing after the checks are complete.

8 In the Report File text box, specify the name and the location of the DRC file to be created.

For the current design example, specify the filename as `fulladd.dsn`.

9 Click OK.

After the checks are done, the DRC report is displayed in the format shown below.

```
Checking Pins and Pin Connections
-------------------------------------------------
Checking Schematic:  FULLADD
-------------------------------------------------
Checking Electrical Rules
Checking for Unconnected Nets
Checking for Invalid References
Checking for Duplicate References
Check Bus width mismatch
-------------------------------------------------
Checking Schematic: HALFADD_A1 HALFADD
-------------------------------------------------
Checking Electrical Rules
```

```
Checking for Unconnected Nets
Checking for Invalid References
Checking for Duplicate References
Check Bus width mismatch
-------------------------------------------------
Checking Schematic: HALFADD_B1 HALFADD
-------------------------------------------------
Checking Electrical Rules
Checking for Unconnected Nets
Checking for Invalid References
Checking for Duplicate References
Check Bus width mismatch
```

## Summary

This chapter covered the steps for creating both flat and hierarchical designs using OrCAD Capture. In the process, you were introduced to basic design creation tasks, such as creating projects, adding libraries to a project, placing parts, and editing property values.

## What's next

In the next chapter, *Simulating a design*, you will use PSpice for simulating the schematic design created in this chapter. You will be introduced to various types of simulations and their need in the PCB design cycle.

## Recommended reading

For more information about OrCAD Capture, see *OrCAD Capture User's Guide* and Capture online help. To know more about OrCAD Unison flow, see the *OrCAD Unison Suites Flow Guide*.

# Simulating a design

# 3

This chapter consists of the following sections:

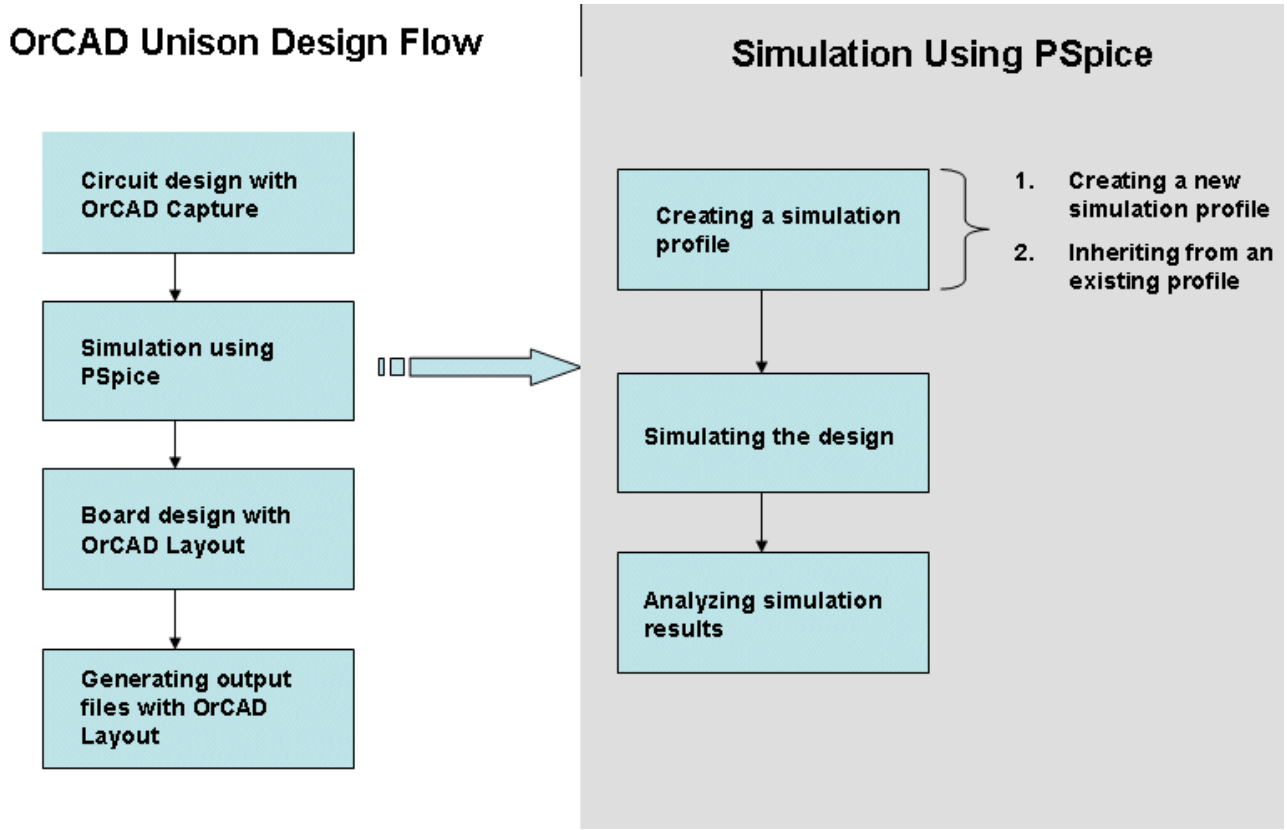
# Objective

PSpice is a simulator provided by OrCAD and can be used to simulate both analog and digital circuits. PSpice simulator is closely integrated with OrCAD Capture to provide you with a rapid design-and-simulate iterative cycle. Using PSpice, you can explore various design configurations before committing to a specific implementation.

In this chapter, you will use PSpice to simulate the full adder design that you created in Chapter 2, Creating a schematic design using OrCAD Capture. In this chapter, you will also learn about the various types of analysis that can be performed using PSpice.

# Simulation using PSpice

PSpice models the behavior of a circuit containing any mix of analog and digital devices.



To simulate a design, PSpice needs to know about:

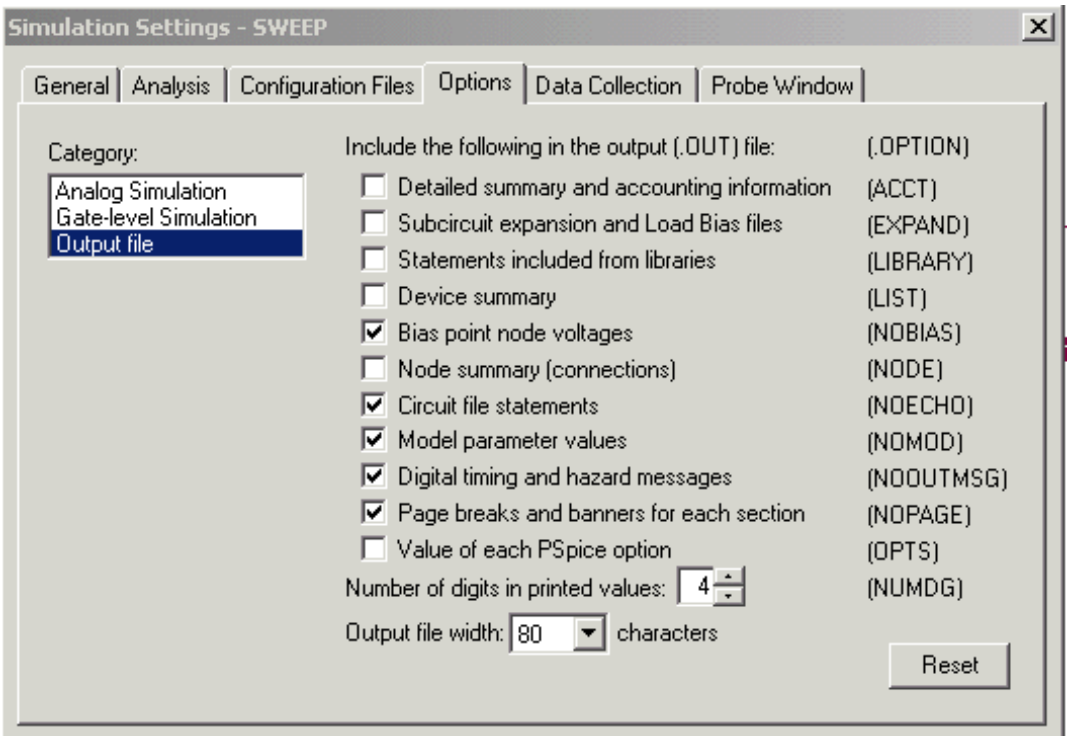
- the circuit topology
- the analysis type
- the simulation models that correspond to the parts in your circuit
- the stimulus definitions to test with

## Files generated by PSpice

After reading various data files and any other required inputs, PSpice starts the simulation. As the simulation progresses, PSpice saves the simulation results in two files, the Waveform data file and the PSpice output file.

- **Waveform data file**: The data file contains simulation results that can be displayed graphically. PSpice reads this file and displays waveforms reflecting circuit response at nets, pins, and parts that you marked in your schematic (cross-probing).
- **PSpice output file**: This is a user-configurable file. Depending on the options specified by the user, this file may or may not contain any information. To configure the

output file, you can use the Options tab in the Simulations Settings dialog box, as shown in the figure below.




For detailed description of the `.OPTION` command, see *PSpice Reference Guide*.

For more information on Files needed and generated by PSpice refer to *PSpice User's Guide, Chapter 1, Things You Need to Know.*

## Analysis types

You can perform the following types of circuit analysis using PSpice:

- DC Analysis
- AC Analysis
- Transient Analysis
- Advanced Analysis

## DC analysis

DC Analysis includes the following:

### DC Sweep analysis

The DC sweep analysis causes a DC sweep to be performed on the circuit that allows you to sweep a source (voltage or current), a global parameter, a model parameter, or the temperature through a range of values. The bias point of the circuit is calculated for each value of the sweep.

To run a DC sweep or small-signal DC transfer analysis, you need to place and connect one or more independent sources and then set the DC voltage or current level for each source.

### Bias Point analysis

The bias point is calculated for any analysis whether or not the Bias Point analysis is enabled in the Simulation Settings dialog box.

### DC Sensitivity analysis

DC sensitivity analysis calculates and reports the sensitivity of one node voltage to each device parameter for the following device types:

- resistors
- independent voltage and current sources
- voltage and current-controlled switches
- diodes
- bipolar transistors

For more information on each type of DC analysis, refer to *PSpice User's Guide, Chapter 9, DC Analyses*.

## AC analysis

AC analysis includes the following:

### AC Sweep analysis

AC sweep is a frequency response analysis. PSpice calculates the small-signal response of the circuit to a combination of inputs by transforming it around the bias point and treating it as a linear circuit.

### Noise analysis

When running a noise analysis, PSpice calculates and reports the following for each frequency specified for the AC Sweep/Noise analysis:

- Device noise is the noise contribution propagated to the specified output net from every resistor and semiconductor device in the circuit. For semiconductor devices, the device noise is also broken down into constituent noise contributions where applicable.
- Total output and equivalent input noise

For more information on each type of AC analysis, refer to PSpice User's Guide, Chapter 10, AC Analyses

## Transient analysis

A transient analysis calculates the behavior of the circuit over time.

For more information on transient analysis, refer to *Chapter 12, Transient Analysis* in the *PSpice User's Guide*.

Besides the analysis types discussed above, you can use PSpice to perform some more analyses that help you evaluate and enhance the performance of your circuit. These analyses cannot be performed independently, but you can configure the

simulation profile to run these analyses along with Transient, AC, or DC analysis. These are:

- Parametric analysis
- Temperature analysis
- Monte Carlo analysis

### Parametric analysis

Parametric analysis performs multiple iterations of a specified standard analysis while varying a global parameter, model parameter, component value, or operational temperature. The effect is the same as running the circuit several times, once for each value of the swept variable.

### Temperature analysis

For a temperature analysis, PSpice reruns standard analyses set in the Simulation Settings dialog box at different temperatures.

You can specify zero or more temperatures. If no temperature is specified, the circuit is run at 27°C. If more than one temperature is listed, the simulation runs once for each temperature in the list.

For more information on parametric and temperature analysis, see *Chapter 11, Parametric and temperature analysis* of *PSpice User's Guide*.

### Monte Carlo analysis

The Monte Carlo analysis calculates the circuit response to changes in part values by varying all of the model parameters for which a tolerance is specified. This provides statistical data on the impact of variance of a device parameter.

### Worst Case analysis

Worst-case analysis is used to find the worst probable output of a circuit or system given the restricted variance of its parameters. For instance, if the values of R1, R2, and R3 can vary by +-5%, then the worst-case analysis attempts to find the combination of possible resistor values that result in the worst simulated output.

For more information on Statistical analysis, *refer to PSpice User's Guide, Chapter 13, Monte Carlo and Sensitivity/Worst case Analysis*.

## Overview of the full adder design

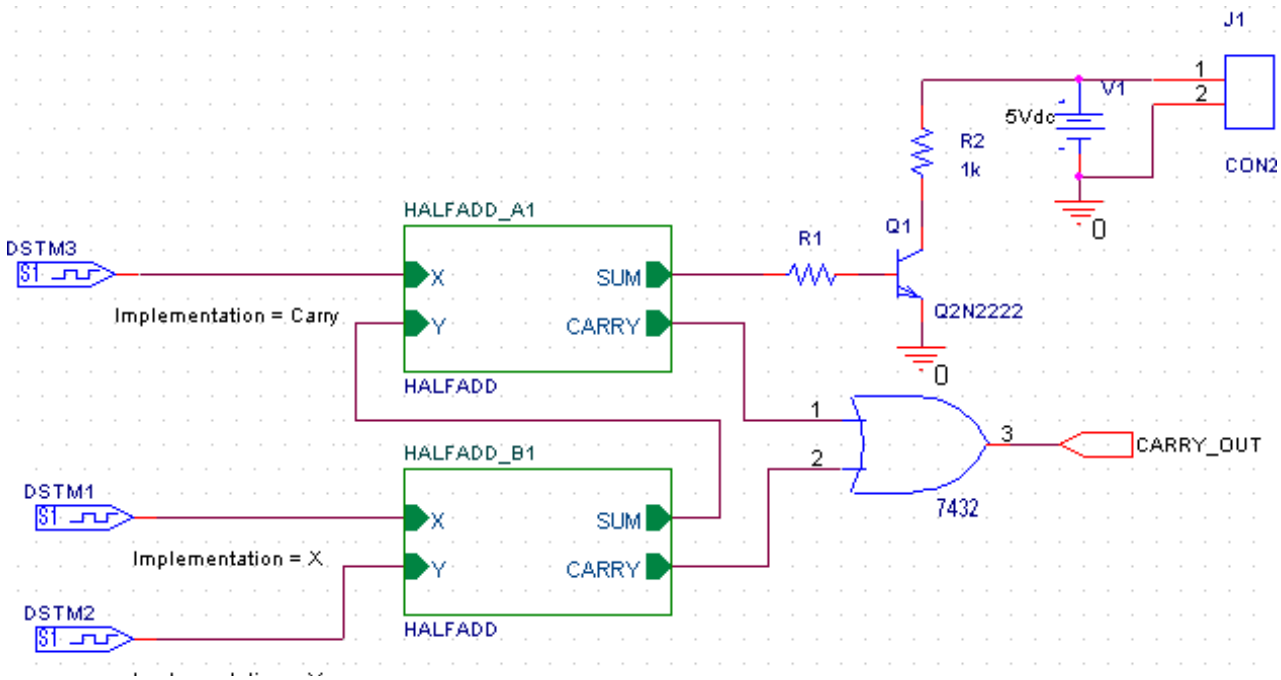
In this chapter, we will simulate the full adder design using PSpice. The full adder design is a complex hierarchical design that has two hierarchical blocks referring to the same half adder design.

To go through the steps detailed in this chapter, you should have the full adder design ready. You can either create the full adder design or use the one provided to you along with the tutorial.

For more information on creating the full adder design, see Chapter 2, "Creating a schematic design,".

To copy the design files provided with the tutorial, unzip the *demotut.zip* file shipped along with the tutorial. The *partial* directory contains files generated at the end of Chapter 2, "Creating a schematic design." Use the files in this directory

only if you want to skip the design creation steps covered in Chapter 2 and directly move on to Chapter 3.



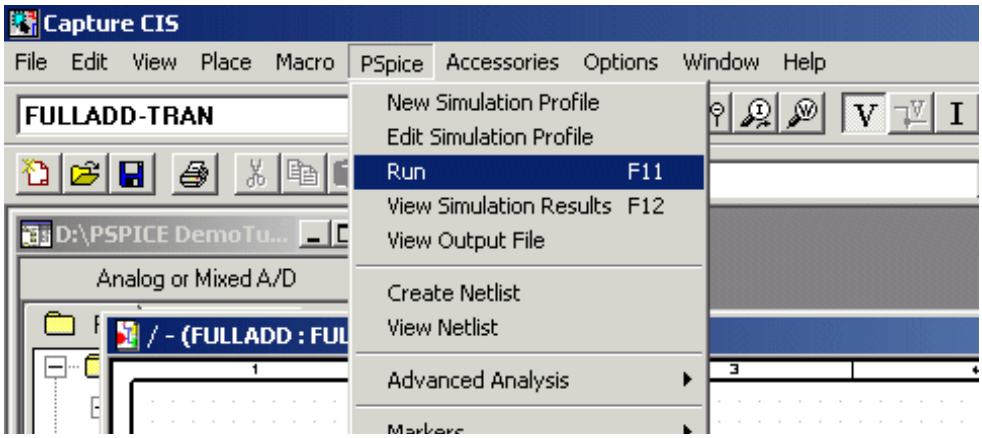

# Running PSpice

To provide PSpice with information about the type of simulation you wish to perform and the resources to be used in your simulation, you must create a simulation profile before you can start a PSpice simulation. A simulation profile saves your simulation settings for an analysis type so that you can reuse them easily.

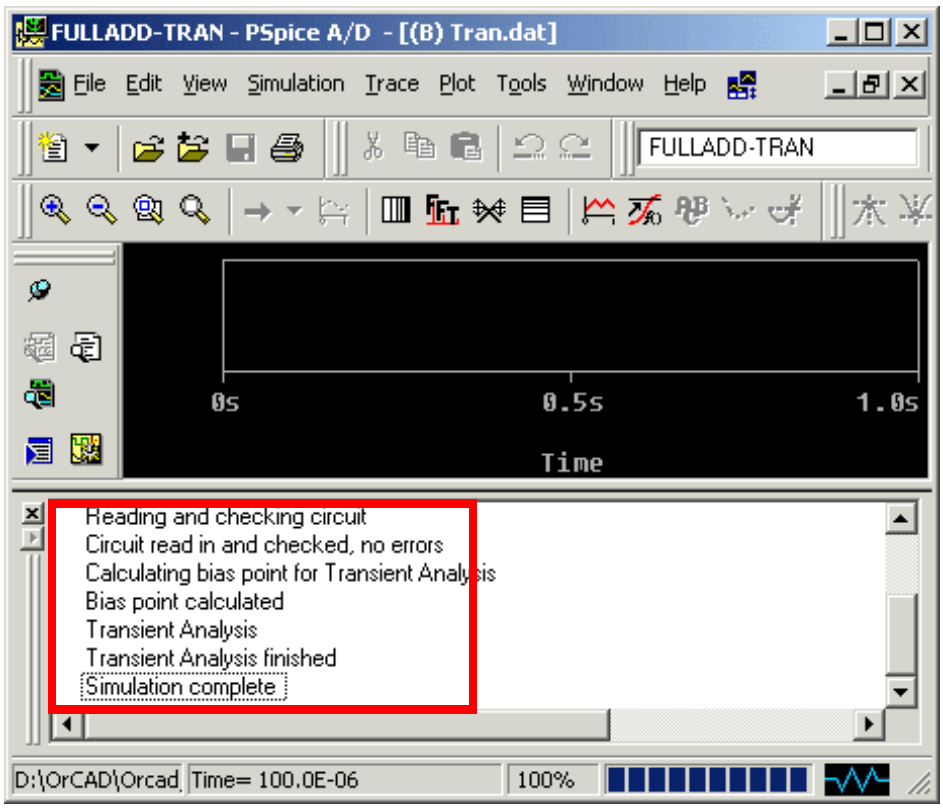
In this section, we will use the TRAN.sim profile to perform transient analysis on the full adder circuit.

For more information on creating the TRAN.sim profile, see Getting your design ready for simulation on page 41.

1 To simulate the design, choose *Run* from the *PSpice* menu in OrCAD Capture.




The PSpice Netlist Generation progress box appears indicating that the PSpice netlist is being generated. After the netlist generation is complete, the design is simulated and PSpice is started. The Output window in PSpice indicates that the simulation is complete.



Though the simulation is complete, the Probe window does not yet display any waveform that might help you analyze the circuit behavior and determine the validity of your design.

## Viewing Output Waveforms

After simulating a design using PSpice, you can plot the output waveforms in the Probe window. This will help you visualize the circuit behavior and determine the validity of your design. You can analyze the output waveforms and evaluate your circuit for performance analysis and data comparison from multiple files.

Using the Probe window, you can:

- view simulation results in multiple Probe windows
- compare simulation results from multiple circuit designs in a single Probe window
- display simple voltages, currents, and noise data
- display complex arithmetic expressions that use the basic measurements
- display Fourier transforms of voltages and currents, or of arithmetic expressions involving voltages and currents
- for mixed analog/digital simulations, display analog and digital waveforms simultaneously with a common time base
- add text labels and other annotation symbols for clarification

For PSpice to display output waveforms in the Probe window, you need to perform at least one of the following steps.

- Place markers
- Add Plot Window template
- Add complex traces

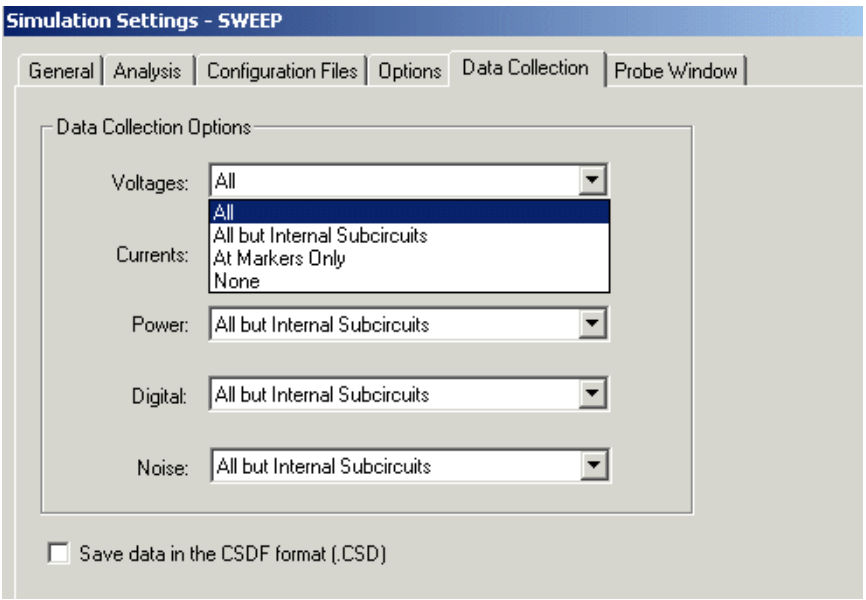
## Place markers

You place markers in your circuit design in Capture to indicate the points where you want to see simulation waveforms displayed in PSpice.

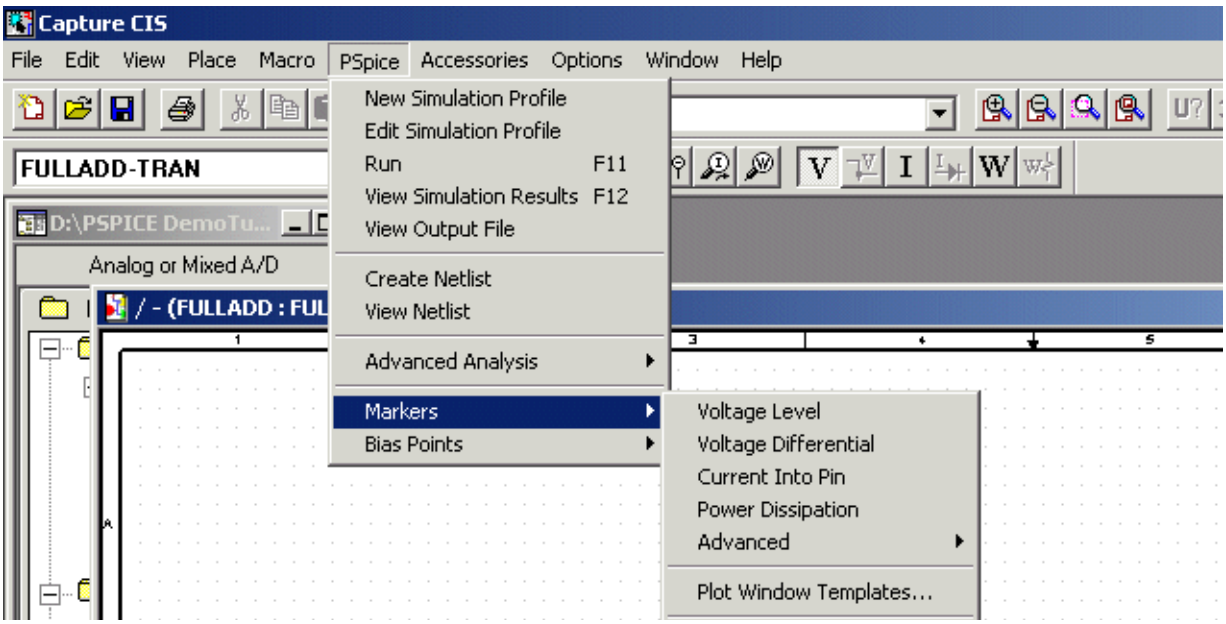
You can place markers:

- before simulation to limit results written to the waveform data file, and automatically display those traces in the active Probe window.
- during or after simulation, to automatically display traces in the active Probe window.

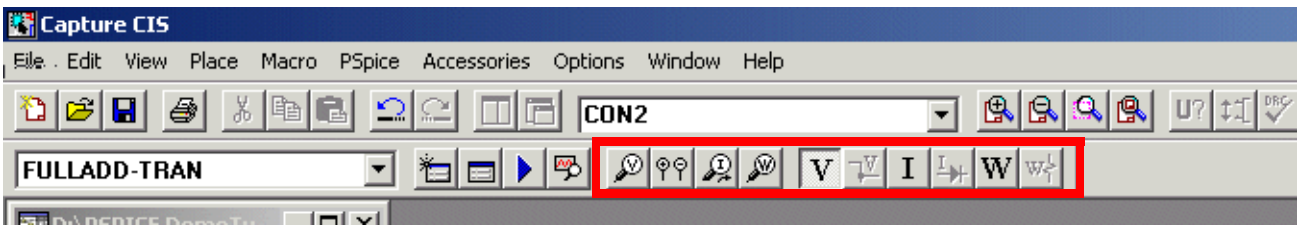
**Note:** You can control the trace display for any of parameter by using the Data Collection tab. For example, if the None option is selected, PSpice will not display any waveform at the point where a marker is placed.



To add markers, from the *PSpice* menu in Capture, choose *Markers*.




You can also use the buttons provided on the Standard toolbar to add markers.

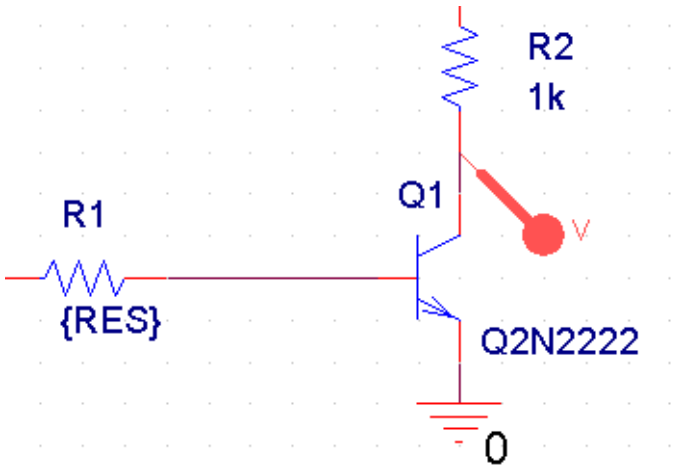



We will now modify the full adder design in Capture by adding Voltage markers to view the output waveforms in the Probe window.

1 From the *PSpice* menu in Capture, choose *Markers* and then select *Voltage Level*.

**Note:** Alternatively, you can click on the Voltage/Level Marker button on the toolbar.

2 Place the marker between transistor Q1 and resistor R2, as shown in the figure given below.




3 To view the output waveform at the marker location, double-click the marker.

The output waveform appears in the Probe window in PSpice. See Figure 3-1 on page 60.

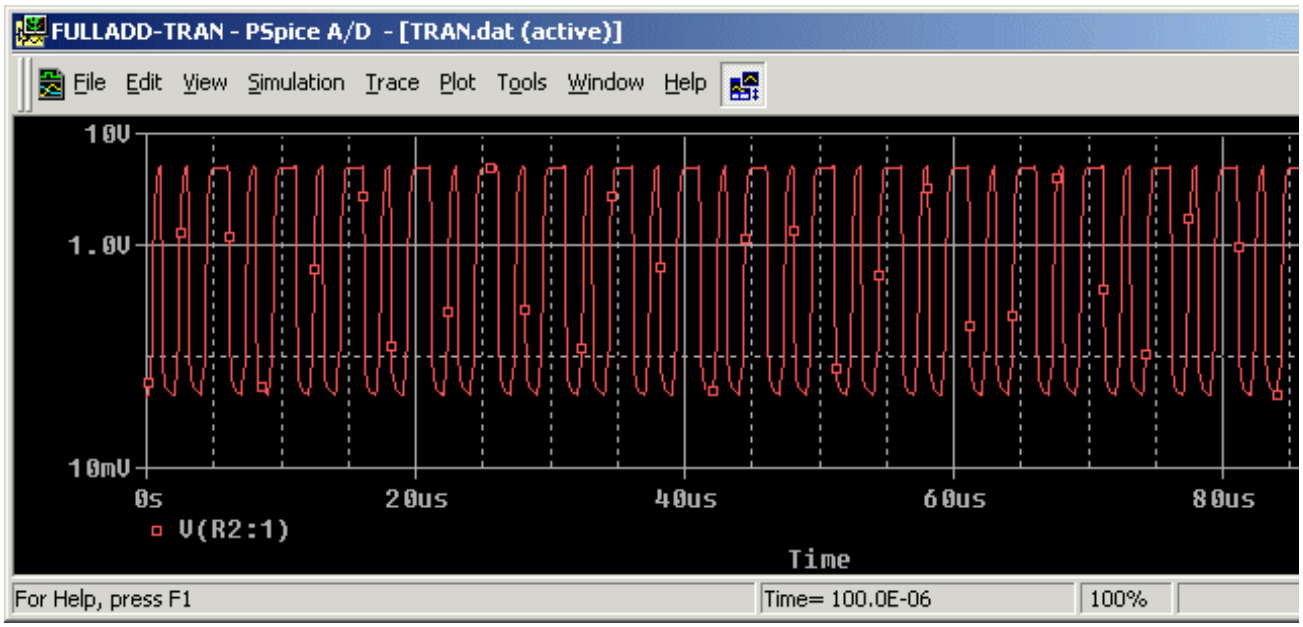



**Figure 3-1 Simulation results for TRAN.sim profile**

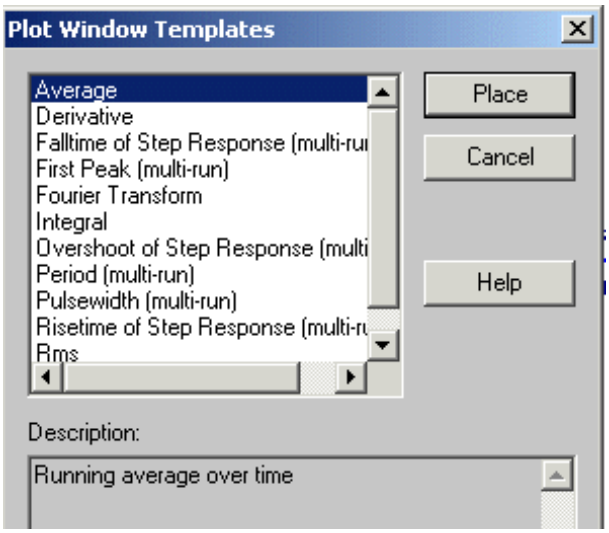
**Note:** If you add markers before simulating the design, the output waveforms are displayed automatically in the Probe window after the simulation is complete.

## Add Plot Window template

In addition to markers, you can place Plot Window Template markers in Capture. A Plot Window Template marker will restore the associated template when you run the simulation in PSpice.

The analysis type defined in the profile will determine the type of template that will be loaded.

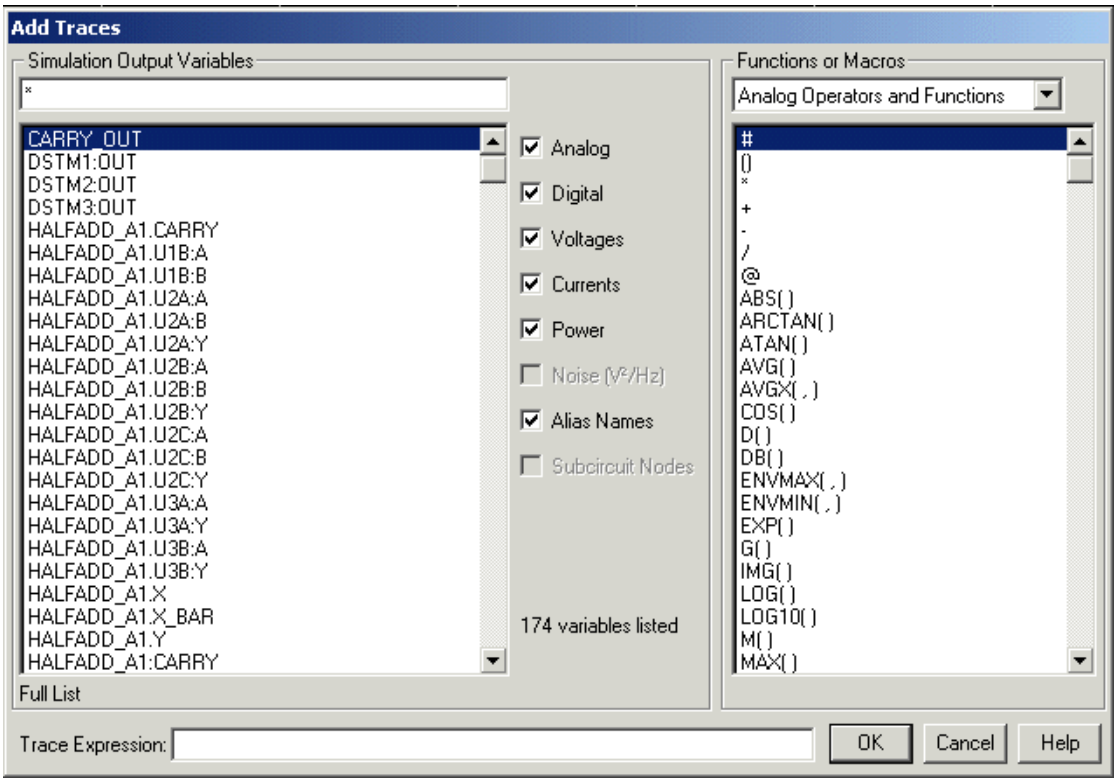
To place a plot window template marker, select *Markers* from the *PSpice* menu, and then select *Plot Window Templates*.




## Add complex traces

By default, the waveforms that PSpice displays are the simple voltages, currents, and noise data from your circuit. Using the *Trace* menu in PSpice, you can add traces that are complex arithmetic expressions that use the basic measurements,

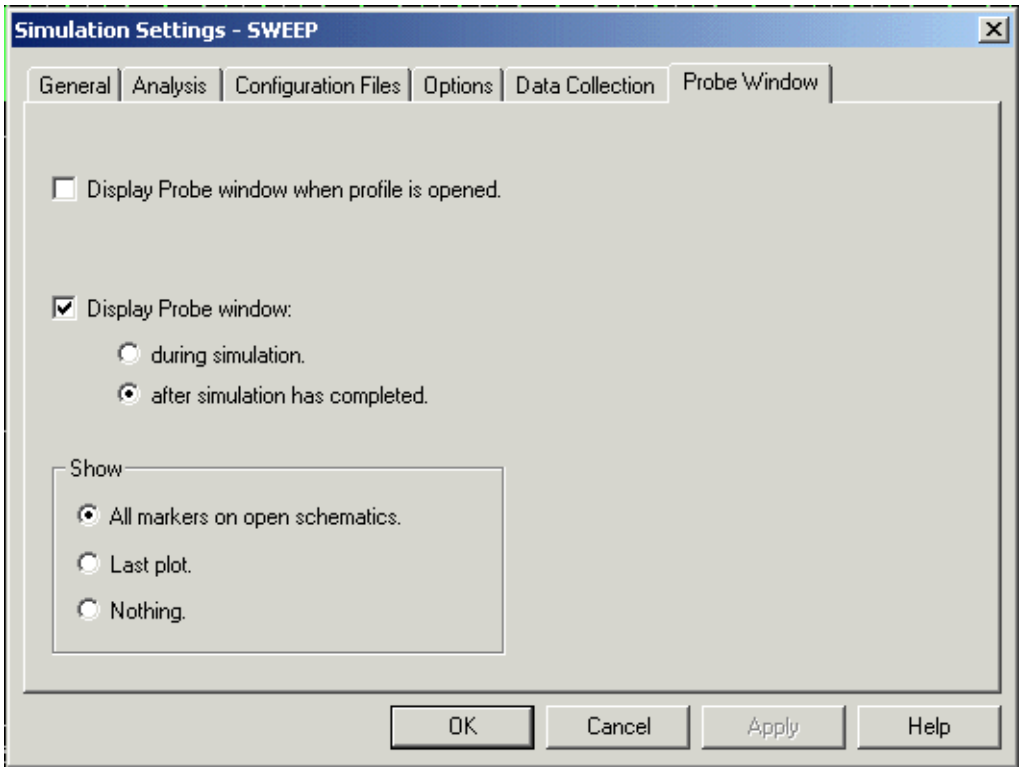
such as Fourier transforms of voltages and currents and arithmetic expressions involving voltages and currents.




## Configuring the Probe window

Using the *Plot* menu in PSpice, you can control the settings for the X- and Y-axis in the Probe windows. Using the *Plot* menu, you can also customize the grid settings in the Probe window and add text labels and other annotation symbols to your traces. You can also configure the way you want to view

the waveforms by defining display settings on the Probe Window tab in the Simulation Settings dialog box.




# Performing parametric analysis

In this section, you will perform the Parametric Sweep analysis on the full adder design. You will evaluate the influence of varying base resistance on the switching characteristics of the transistor.

To do this, you need to perform the following steps:

- Modify the full adder circuit by changing the value of resistor R1 to a variable {RES}.
- Place a PARAM part to declare values of the parameter {RES}.
- Create a new simulation profile or modify the existing profile to set up the parametric analysis.

In this example, there will be multiple simulation runs, one for each value of resistor R1. After the analysis is complete, you can analyze output waveforms for the analysis runs using PSpice A/D.

## Adding a variable circuit parameter

### Changing the value of R1 to the expression {RES}

1. Open the full adder design, `FullAdd.opj`, in OrCAD Capture.
2. To display the Property Editor window for R1, double-click resistor R1.
3. In the Value text box, replace the original value of 1K with {RES}.
4. Click OK to save the modifications.

**Note:** Curly braces indicate that the variable or the expression within the braces will evaluate to a numerical value.

### Adding a PARAM part to the FULLADD design

1. From the *Place* menu in Capture, choose *Part*.
2. Using the Place Part dialog box, add SPECIAL.OLB to the FULLADD project.
3. In the Libraries list box, select `SPECIAL.OLB`.
4. From the Part List list box, select `PARAM` and click OK.
5. Place an instance of the PARAM part on the schematic page.
6. Double-click the PARAM part to display the Property Editor and click New Row.

   The Add New Row dialog box appears.

   **Note:** In the Property Editor window, you can also display properties names as column headings. In such cases, to add a new property, click the New Column button. The

Add New Column dialog box will appear.

7 In the Name text box, enter `RES`, without curly braces.

8 Specify the value as 10K and click OK.

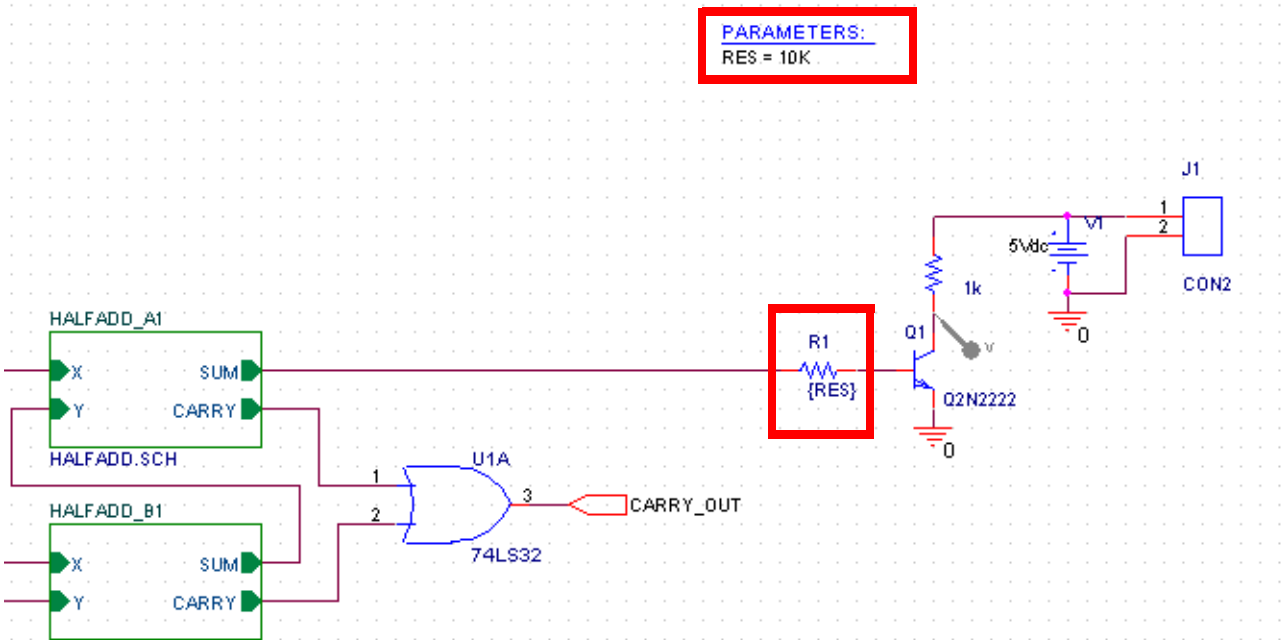
This creates a new property for the PARAM part, as shown by the new column labeled RES in the Property Editor window.

9 Select the new cell RES and click Display.

10 In the Display Format frame, select *Name and Value* and click OK.

11 Click Apply to update all the changes to the PARAM part.

12 Close the Property Editor window.



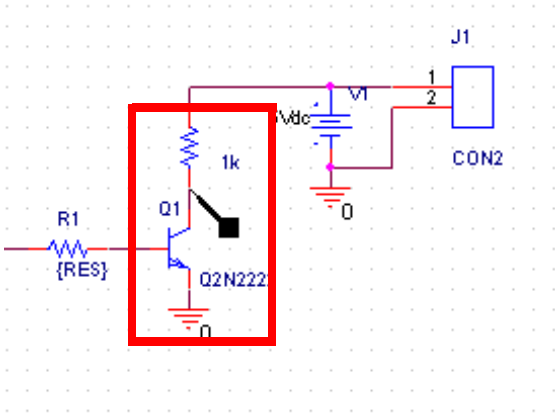

You can view the changes on the schematic page.

**Note:** For more information about using the Property Editor, see the *OrCAD Capture User's Guide*.

## Adding a Plot Window Template marker

In this section, we will add a Plot Window Template marker to the circuit and observe the change in the output for different values of R1.

1. Remove the voltage marker added to the schematic design in the Place markers section.
2. From the *PSpice* menu in Capture, choose *Markers* and then select *Plot Window Template*.
3. Select the *Risetime of Step response* template marker from the Plot Window Templates dialog box and click Place.
4. Place the marker between transistor Q1 and resistor R2, as shown in the figure given below.




## Setting up parametric analysis

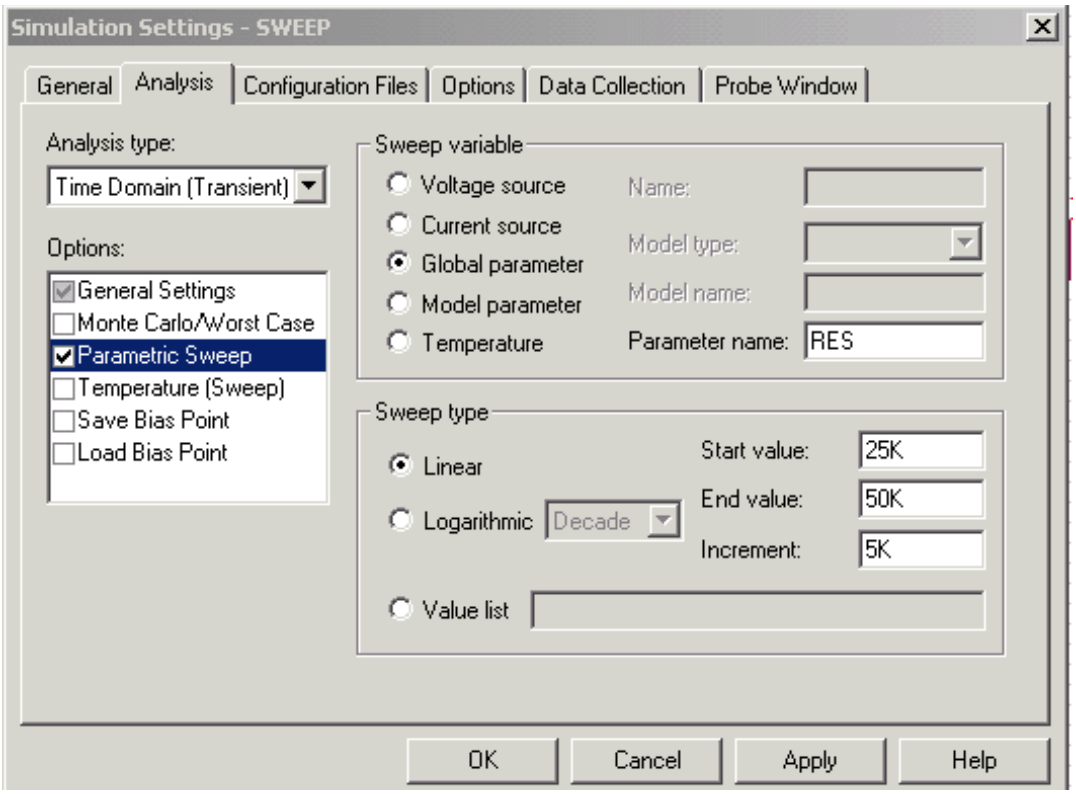
In this section, we will use the FULLADD-SWEEP simulation profile to set up the parametric analysis. This simulation profile has been created by inheriting the settings from the FULLADD-TRANS profile. See Creating a simulation profile from an existing profile on page 42.

The simulation profile created in the Creating a simulation profile from an existing profile section, does not cover the settings for the parametric analysis. Therefore, we need to modify the FULLADD-SWEEP simulation profile. To do this,

you first make SWEEP the active simulation profile in Capture and then open the profile for modifications.

1. In Capture, select FULLADD-SWEEP from the Active Profile drop-down list box.
2. From the *PSpice* menu, choose *Edit Simulation Profile*.

   The Analysis tab of the Simulation Settings dialog box appears.
3. Select the Parametric sweep check box in the Options list box.
4. Select the *Global parameter* option button under the Sweep variable. This sets the value to the sweep value and all expressions are re-evaluated.
5. Type `RES` in the Parameter name text box.
6. Type `25K`, `50K`, and `5K` in the Start value, End value, and Increment text boxes, respectively.
7. Click OK.

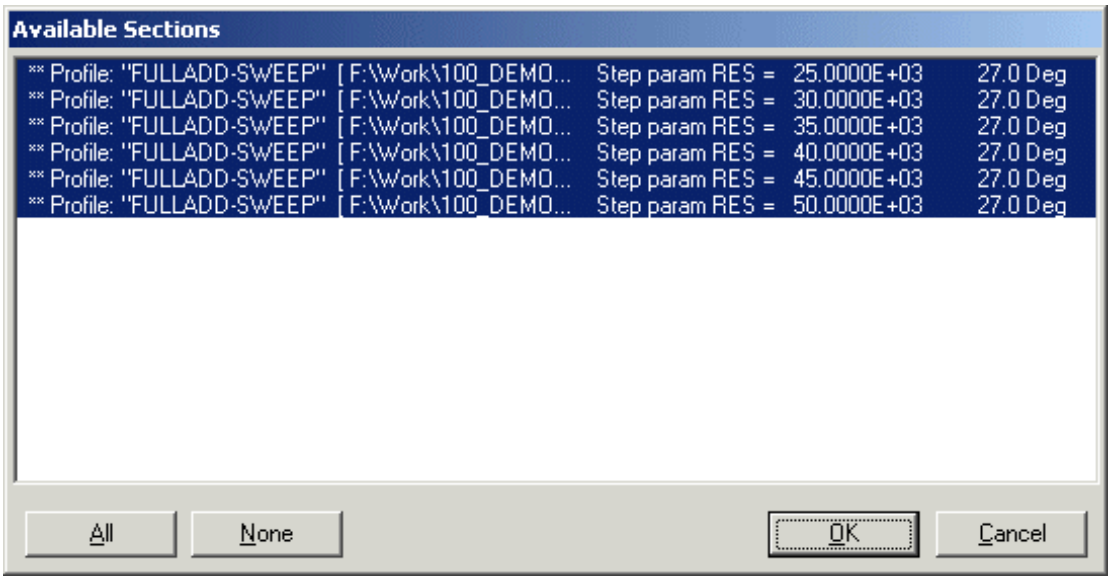


**Note:** Instead of creating a new profile in OrCAD CApture, you can create a new simulation profile in PSpice also by inheriting settings from an existing profile. The new profile will work with your circuit design and can also be modified within PSpice. To modify a simulation profile in Capture, you use the Edit Simulation Profile command from the PSpice menu. In PSpice, use the Edit Profile command from the Simulation menu.

## Running the simulation

To run the Parametric analysis, choose *Run* from the *Simulation* drop-down menu.

When the simulation is complete, the Simulation complete message appears in the output window, and the Available Sections dialog box appears as shown in the figure below.




This dialog box appears for all multi-run analyses.

Select the runs for which you want to display the data and click OK. The simulation results are shown in Figure 3-2 on page 69.

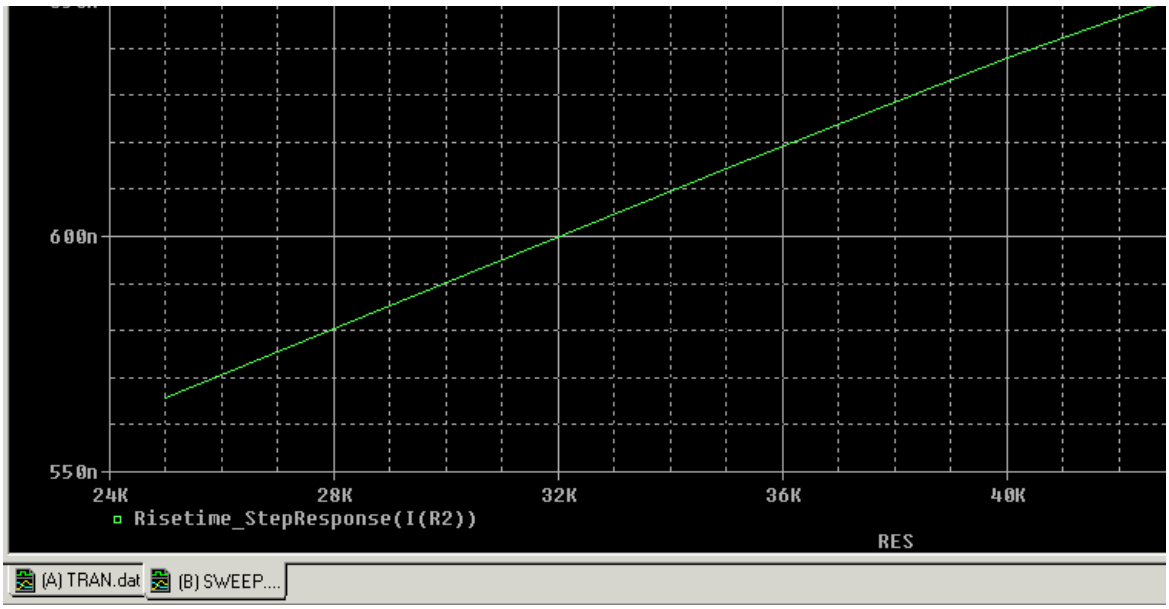



**Figure 3-2 Simulation results for Parametric Analysis**

To read more about Parametric Analysis, see the *Parametric analysis* section in *Chapter 11, Parametric and temperature analysis* of the *PSpice User's Guide*.

*Tip*

You can use the Performance Analysis Wizard to create a Performance Analysis trace for evaluating the performance of your circuit. To know more about the Performance Analysis wizard, see *Chapter 11, Parametric and temperature analysis* of the *PSpice User's Guide*.

## Exporting output waveforms

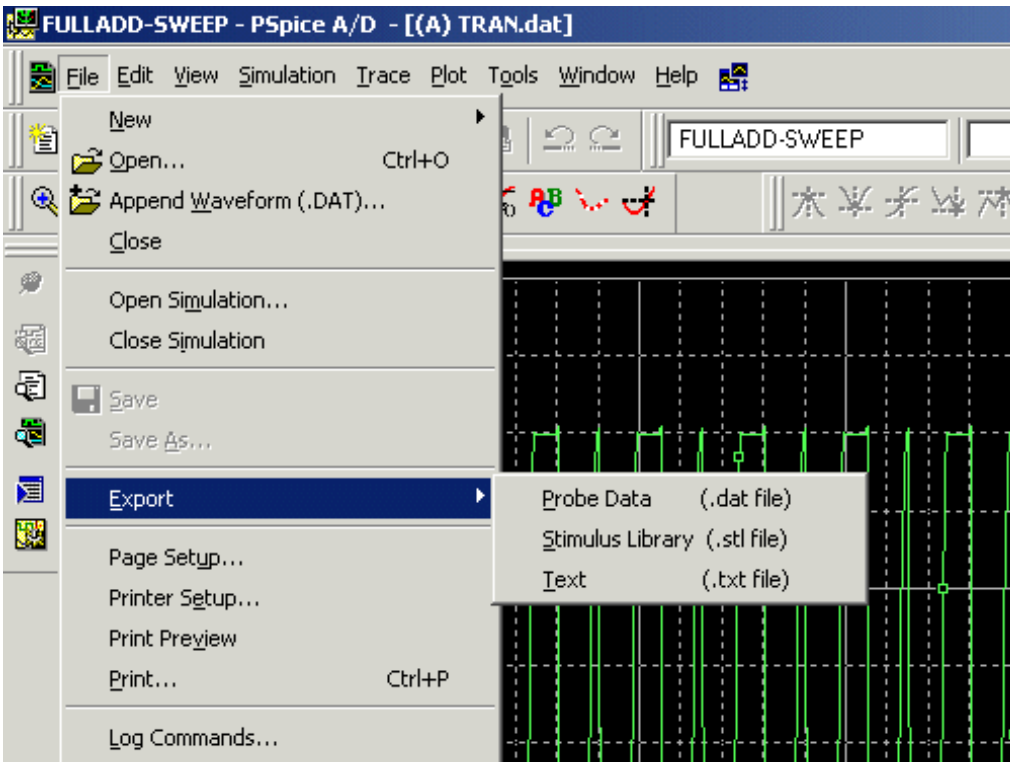
You can export the output waveforms in the following formats:

- `.dat` file
- `.stl` file

- `.txt` file

To export the output waveform:

– From the *File* menu in PSpice, select *Export* and then select the desired format.




## Summary

This chapter covered the steps for simulating the full adder design using OrCAD PSpice. In this chapter, you were introduced to various tasks involved in the simulation process, such as placing markers and templates, modifying a simulation profile, and analyzing simulation results.

## What's next

In the next chapter, *Board design using OrCAD Layout*, you will use OrCAD Layout to create a PCB board for the full adder design.

# Recommended reading

For more information about PSpice, see *PSpice User's Guide* and PSpice online help. To know more about OrCAD Unison flow, see *OrCAD Unison Suites Flow Guide.*

# Board design using OrCAD Layout

# 4

This chapter consists of the following sections:



## Overview

The OrCAD Layout place-and-route tool offers PCB designers the power and flexibility to create and share PCB data and constraints across the design flow. It is an ideal tool for individuals and small-to-medium design teams creating printed circuit boards from prototype to production.

OrCAD Capture supports cross-probing with OrCAD Layout. This implies that you can select an item in Capture and see the

corresponding item highlighted in OrCAD Layout, and conversely. For example, when you select a net in Capture, corresponding net in the PCB board gets highlighted. In case of components such as a gate or a transistor, the corresponding package in the board is highlighted.

# Objective

In this chapter, you will use OrCAD Layout to take the full adder design created in Chapter 2, Creating a schematic design, to a PCB board. This chapter details some of the common tasks involved in PCB layout. In the process, you will also use cross-probing between Capture and Layout.

## Tutorial design

To go through the steps detailed in this chapter, you should have the full adder design ready. The full adder design used in this tutorial is a hierarchical design. It has two instances of the HALFADD hierarchical block.

You can either use the design you created in Chapter 2, Creating a schematic design or if you want to skip the design creation section, you can pick up the design files shipped with the tutorial.

## Installing design example

The design files for the full adder design are available in the `demotut.zip` file shipped along with the tutorial.

Unzip the `demotut.zip` file and extract it to an empty directory, say `orcad_demos`. On extracting the `demotut.zip` file, you will find two sub-directories, `partial` and `complete`, created in the `orcad_demos` directory.

The `partial` directory contains files generated at the end of Chapter 2, “Creating a schematic design.” Use the files in this directory only if you want to skip the design creation steps covered in Chapter 2 and directly move on to Chapter 4.

The `complete` directory contains all the files generated through all the chapters in this tutorial. You can use the files in the `complete` directory to verify your results.

### Estimated completion time

30 minutes

# Preparations in Capture

To be able to take a design created in Capture to OrCAD Layout, you need to complete some tasks. Some of these tasks are performed in OrCAD Capture while the rest are completed in the OrCAD Layout environment.

The tasks that are to be completed in OrCAD Capture are

- Running DRC
- Creating Layout netlist

## Running DRC

Before taking a design from a schematic editor to a board planner, it is a good idea to run design rules check (DRC). This step is performed in OrCAD Capture. To view the procedure, see Design rules check on page 44.

## Creating Layout netlist

After running the Design Rule Checks, you create the Layout netlist in Capture.

1. In the Project Manager window, select the design file, `fulladd.dsn`.
2. From the *Tools* menu in Capture, choose *Create Netlist*.
3. In the Create Netlist dialog box, select the Layout tab.

4 In the Netlist File text box, type `FULLADD.MNL` as the name for the layout netlist to be created.

5 Click OK.

# Creating a board

Having created the layout netlist, the next step is to create a new board in Layout.

## Launch Layout

– From the Start menu, choose *Programs > OrCAD 10.0 DEMO > Layout Demo*.

## Create the Layout board file

When you create a new board file in OrCAD Layout, you merge the electrical information from the layout netlist (`.MNL`) and physical information from a template file (`.TPL`) or a technology file (`.TCH`) to create a new board design (`.MAX`). Therefore, to be able to create a board file for a new design in Layout, you need to provide a template file and a netlist.

A template (`.TPL`) file describes the characteristics of a physical board. A template can include information, such as the board outline, the design origin, the layer definitions, grid settings, spacing rules, and default track widths.

**Note:** There are some sample board template files provided with the demo version of Layout. These are located in the *<install_dir>\orcad_10.0_demo\tools\layout\data* directory, where *<install_dir>* is the installation location.

A Layout netlist file (`.MNL`) describes the parts and interconnections in a schematic.

A technology file (`.TCH`) can be considered as a subset of the template files. This is because technology files contain information, such as default line width, spacing, grid settings, layer definitions, and via padstacks, but they do not provide any information regarding physical characteristics of a board.

1 From the *File* menu in OrCAD Layout, choose *New*.

The AutoECO dialog box appears.

2 In the *Input Layout TCH or TPL or MAX file* text box, specify the name and the location of the technology file to be used for your board. You can either create your own templates or use existing ones. To view the existing technology files, click the Browse button.

From the list of files, select `2bet_smt.tch` and click Open.

**Note:** `2bet_smt.tch` is the technology file used for moderate design complexity, standard manufacturing, surface mount or mixed-technology boards. The placement grid is 50 mils and route spacing is 8 mils.

*Important*

To know more about the `.TCH` files, see *Technology templates* in the *Layout files and file translation* chapter of the *OrCAD Layout User's Guide*.

3 In the *Input MNL netlist file* text box, specify the location of the `FULLADD.MNL` created in the Creating Layout netlist section.

Note that the *Output Layout MAX file* text box, is automatically populated with the name and the location of the Layout board file, `FULLADD.MAX`.

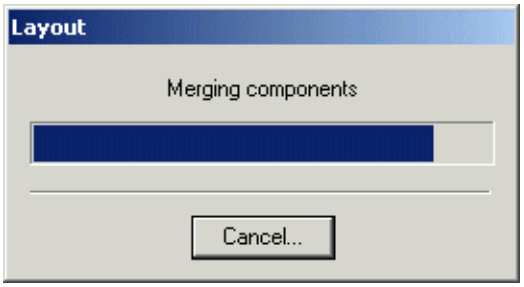
**Note:** A Layout board file (`.MAX`) contains complete physical and electrical information about the board.

4 From the drop-down list in the Options section, select *AutoECO*.

5 To create the Layout board file with the settings specified by you, click ApplyECO.

The Layout progress box appears indicating that the board file is being created. The process of creating a board file will be completed only if the footprint

information is available for all the components in the design.



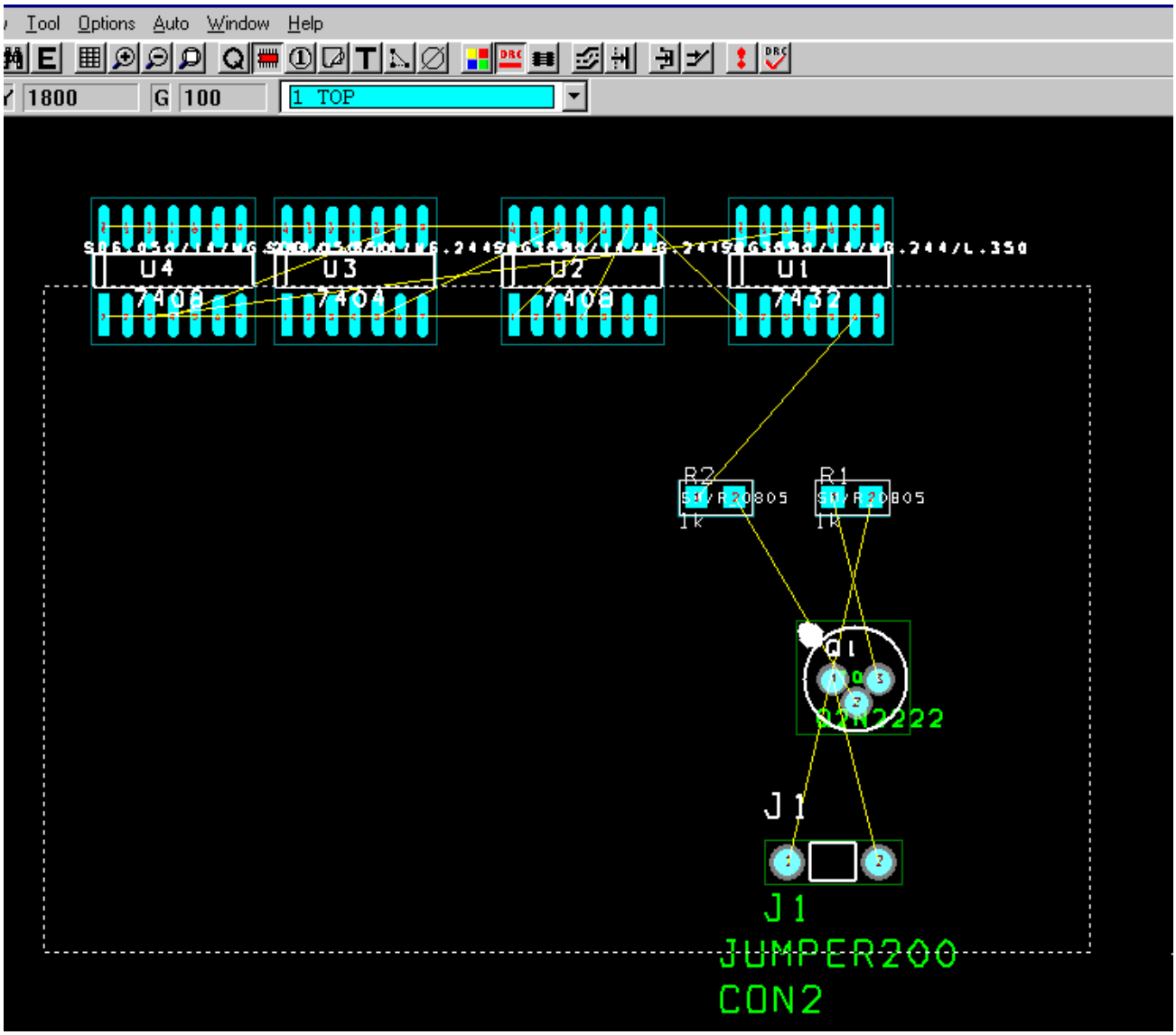

*Important*

If the footprint information for a component is missing, the Link Footprint to Component dialog box appears. To know more, see Adding footprint information on page 79.

6 Once the AutoECO process is complete, the AutoECO dialog box appears with the report. To accept the changes, click the Accept this ECO button.

7 The AutoECO message box appears stating that the process is complete. Click OK.

The layout board file, with components and the connectivity information appears.




## Adding footprint information

You can add footprint information to a component using one of the following OrCAD tools:

- OrCAD Capture

To view how to add footprint information to a component in Capture, see the Adding Layout specific properties section of Chapter 2, "Creating a schematic design,".

- OrCAD Layout

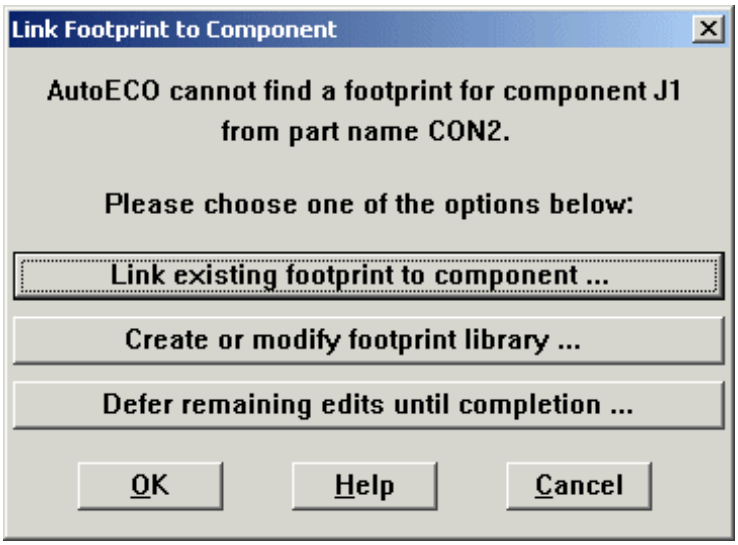
  To add footprint information using OrCAD Layout, see the Adding Footprints section.

*Tip*

When you add footprint information in OrCAD Capture, you need to add the information on all the components individually. OrCAD Layout provides you with an option of adding footprint information to all similar components at one go.

## Adding Footprints

During the AutoECO process, if the footprint information is missing for a component, the Link Footprint to Component dialog box appears.



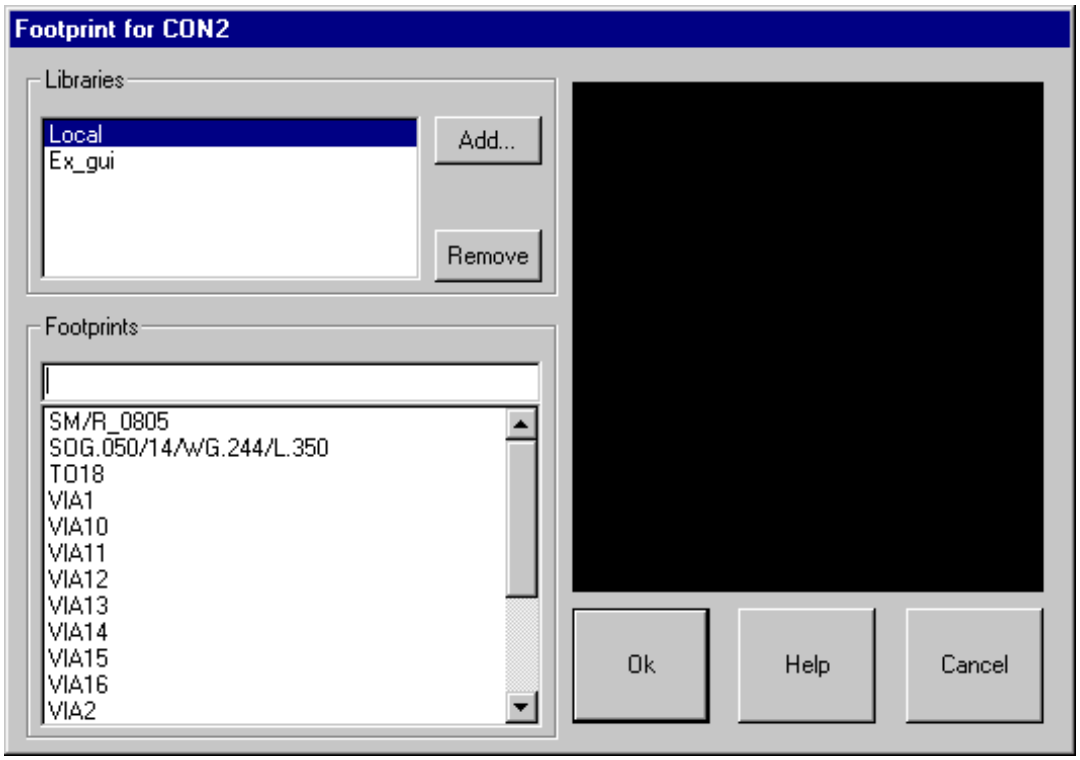

To complete the AutoECO process, you can either add the footprint information by selecting the Link existing footprint to component button or ignore this and continue with the AutoECO process by selecting the Defer remaining edits until completion button.

**Note:** When you select the Defer remaining edits until completion button, an error report with a consolidated list of components with missing footprint information is is generated. This option should be selected when you want to add footprint information using your schematic editor.

In this example, the footprint info for CON2 is missing. To add footprint information using Link Footprint to Component dialog box, complete the following steps:

1 Select the Link existing footprint to component button.

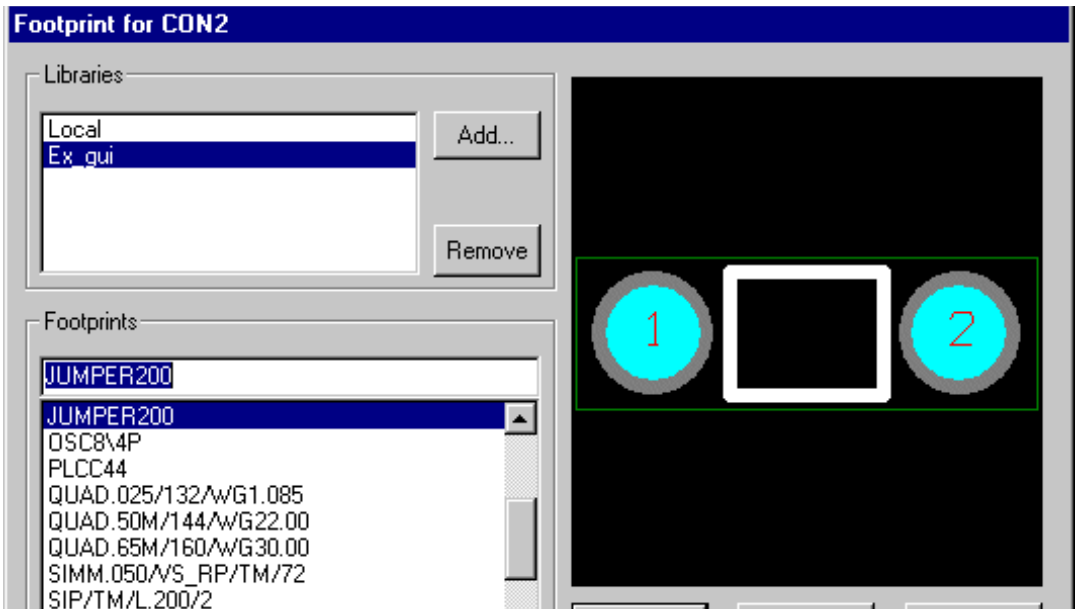
The Footprint for CON2 dialog box appears.




2 From the libraries list box, select `Ex_gui`.

3 From the Footprints list box, select `JUMPER200`.

Selected footprint appears in the preview window.




4 To add the footprint information to the component, click OK.

The footprint information added using the Link footprint to component dialog box, is available only in layout board file. This information is added to the schematic component when you back-annotate the board information on to the schematic.

## Creating a board outline

Layout requires one board outline on the global layer. The board outline defines the boundary of the board. To create a board outline:

1 From the *Tool* menu, select *Obstacle* and then select *New*.

2 To insert the first corner of the PCB board, click the left-mouse button and draw the board outline.

3 Because a board outline must be a closed polygon, Layout automatically begins forming a closed area after you insert the first corner of the board outline, and automatically closes the polygon for you if you don't close it yourself.

Continue clicking the left mouse button to insert corners.

4 Right-click and select *Finish*.

Layout automatically completes the board outline.

## Placing components

After you have created the board outline, you can start placing your components in the board. OrCAD Layout supports both manual placements and auto placements.

*Important*

The auto placement feature is not available in the OrCAD 10.0 demo version of Layout.

In this section, we will use manual placements to create the PCB board for the full adder design. There are different ways in which you can select a component for placement.

### Selecting components using mouse

1 From the toolbar, select the Component Tool button.

2 Select a component with the left-mouse button.

The component attaches to the cursor.

3 Move the component to the desired location.

4 To release the component, right-click and select *End Command*.

**Note:** You can also use the <Esc> key to exit any active command.

5 Press the <F5> key to refresh your screen.

**Note:** For proper placement, you can rotate the components. To do this, right-click on the component and select *Rotate*. Alternatively, press the <R> key.

### Selecting components using part reference

To select a component with a particular part reference:

1. Right-click and choose *Select Any*.

   The Component Selection Criteria dialog box appears.

2. In the Ref Des field, type `U2` and click OK.

   The component with the part reference value as U2 is attached to the cursor.

3. Move the component to the desired location.

4. Right-click on the board and choose *End Command*.

### Queuing components

To select all the components that satisfy a criterion and then place them one after another:

1. Right-click on the board and select *Queue for placement*.

   The Component Selection Criteria dialog box appears.

2. In the Ref Des text box, specify the reference designator as `U*` and click OK.

   When you specify the reference designator as U*, all the components that have reference designators beginning with the alphabet U are selected for placement.

3. To place the component, right-click and choose *Select Next*.

   **Note:** Alternatively, you can press the `<N>` key.

   The component U1 gets attached to the cursor.

4. Click the location where you want to place the component.

5. To place the next component, press the `<N>` key.

6. Right-click and select *End Command*.

7. Save the board.

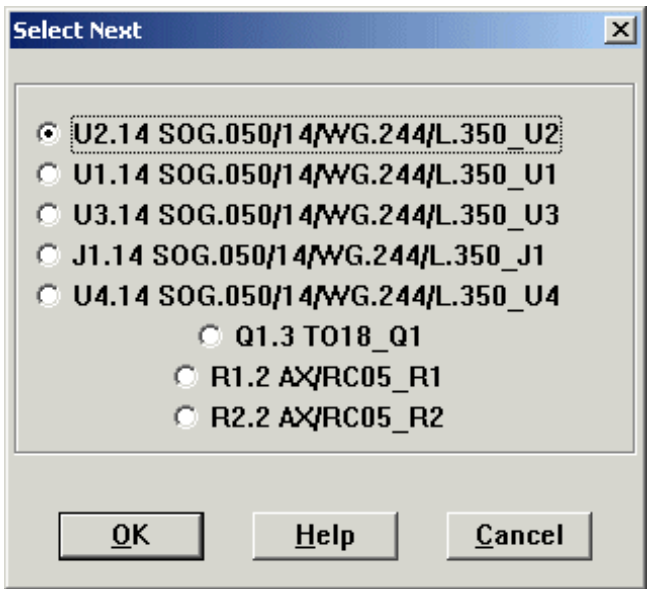
## Selecting the next component to be placed

When you use reference designators to place the components, you can view and select the next component to be placed. To do this, use the following sequence of steps:

1. From the toolbar, select the Component Tool button.
2. Right-click on the board, select *Queue for placement*.

   The Component Selection Criteria dialog box appears.
3. To ensure that all the components are selected, specify the reference designator as * in the Ref Des text box, and click OK.
4. Right-click and select *Place*.

   The Select Next list box appears with the names of all the components yet to be placed.




5. Select the component you want to place first and click OK.
6. To select the next component for placement, right-click with in the board outline and select *Place.*

   The component list is displayed once again.
7. Select the component to be placed and click OK.

8 Complete the component placement and save the board.

**Note:** To know more about placing components, see *Chapter 9, Placing and editing components* of the *OrCAD Layout User's Guide*.

*Tip*

OrCAD Capture allows you to specify the exact location of a component on a PCB during the schematic design stage itself. You can achieve this by adding the COMPLOC property to a schematic component. Similarly, you can use the COMPGROUP property in the schematic to define a group of parts that should be placed together on the board. To know more about these properties, see *OrCAD Layout User's Guide*.

While doing manual placements, you can use various types of interactive placement techniques, such as matrix placement, group placement, and cluster placements. To know more about these, see *OrCAD Layout User's Guide*.

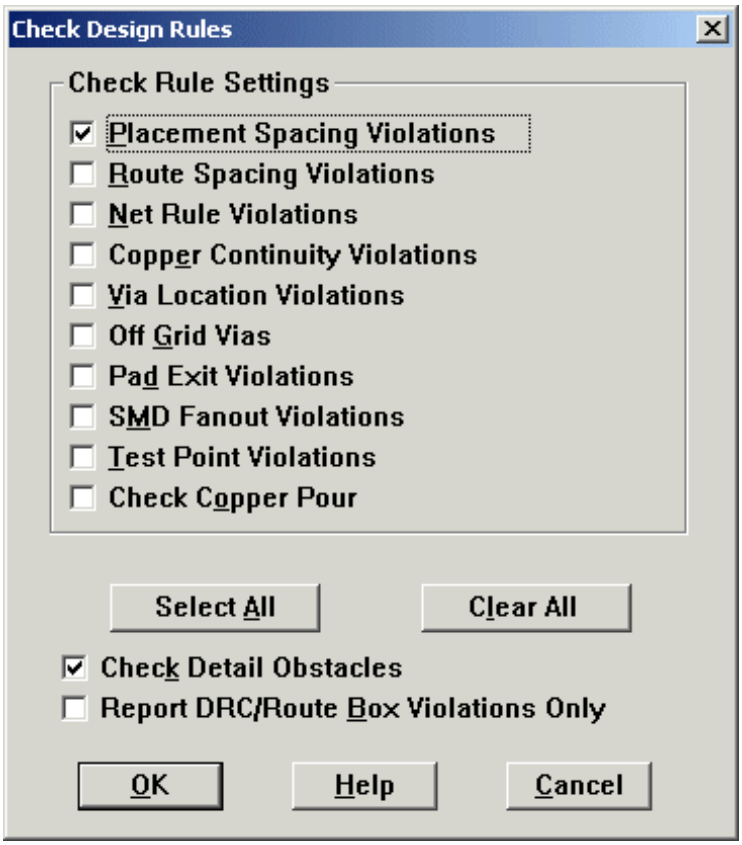
## Design rules check

Whenever you use manual placements to place components, it is a good idea to run a check to ensure that component placement has been done properly and there are no spacing violations.

1 From the *Auto* menu in Layout, choose *Design Rule Check*.

The Check Design Rules dialog box appears.

2 Specify the checks that you want to run. For the full adder design, select the Placement Spacing Violations check box.




3 Click OK.

Layout checks the board for violations and marks any errors with circles.

# Routing

After completing the board placement, you can route the full adder board to complete the electrical connections between components. OrCAD Layout supports both manual routing and Autorouting. The general use model is to first route the critical nets manually, lock them and then autoroute the rest of the board.

## Manual routing

The steps involved in the manual routing process are as follows:

- Check the board outline, via definitions, routing and via grids
- Load a routing strategy file
- Route power and ground
- Fan out surface mounted devices and verify connections to power and ground
- Route the remaining signals using the manual routing tools
- Optimize routing using the manual routing commands
- Check for route spacing violations and check routing statistics

**Note:** To know more about each of these steps, see *Routing the board manually* section in *Chapter 10, Routing the board* of *OrCAD Layout User's Guide*.

### Adding fanouts

It is a good practice to first route critical nets, such as power and ground. For multi-layer boards with surface mounted devices, fanouts can be used to route the power and ground nets.

### Enabling nets for routing

1 Select the View Spreadsheet  button from the toolbar.

2 Select *Nets*.

The Nets spreadsheet appears.

3 Select the Routing Enabled column and right-click.

4 Select *Enable<->Disable*.

All the entries in the Routing Enabled column are changed to NO indicating that the nets cannot be routed.

5 Select the nets named GND and VCC.

6 Right-click and select *Enable<->Disable*.

Entries the Routing Enabled cell for the GND and VCC nets change to Yes.

**Note:** If you now view the board file, only the GND and VCC nets are visible.

7 To edit the net setting, double-click the GND net.

8 In the Edit Net dialog box, click the Net Layers button.

The Layers Enabled for Routing dialog box appears.

9 In the Plane Layers section, select *GND* and click OK.

10 Click OK to close the Edit Net dialog box.

The entry in the Routing Enabled cell for the GND net, changes to Yes*.

11 Similarly, double-click the VCC net.

12 In the Edit Net dialog box, click the Net Layers button.

13 In the Plane Layers section, select *POWER* and click OK.

14 Click OK to close the Edit Net dialog box.

15 Close the spreadsheet.

### Running fanout

1 From the *Auto* menu, choose *Fanout > Board*.

The router generates fanout vias for all surface mount pins attached to the GND and VCC nets.

2 To refresh the screen, press the <F5> key.

All the nets disappear and vias added because of fanout appear.

Open the Nets spreadsheet and enable rest of the nets for routing.

## Routing remaining nets

To manually route the board,

1 Select the Add/Edit Route Mode button from the toolbar.

2 Click on the net to be routed.
The route gets attached to the cursor.

3 Draw the net through the desired path.

4 To change the direction of the routed net, click to end a segment of the net and then change the direction in which you are drawing the net.

5 When you have completed routing, right-click and select *End Command*.

6 To lock a routed net, select the net, right-click on the net, and select *Lock*.

*Tip*

Before manual routing, it is a good practice to keep minimizing the unused nets. To do this, press the <M> key.

## Autorouting using Layout

OrCAD Layout supports autorouting of board, components, and DRC.

Board autorouting implies that the nets on the complete board are routed. Component routing routes only the nets attached to the selected component. DRC routings implies that all the nets within the DRC box defined by the user are routed.

### To autoroute a component

1 From the *Auto* menu, choose *Autoroute > Component*.

2 Select the component that you want to route. All the nets connected to that component are routed.

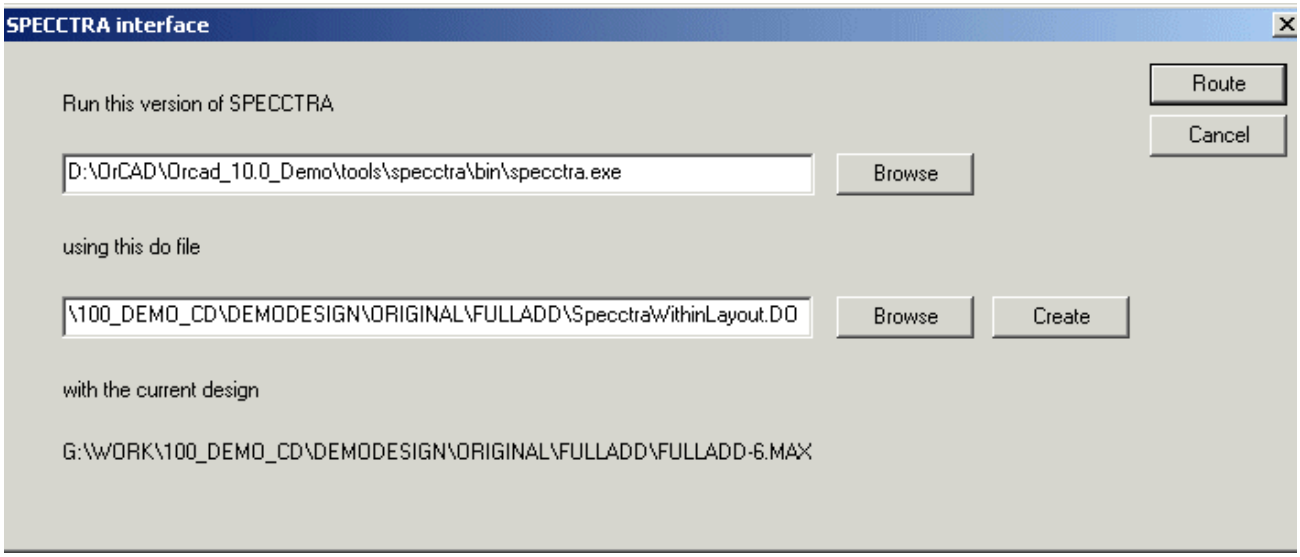
Similarly, to automatically route a complete board, choose *Board* from the *Autoroute* submenu. To autoroute region choose *DRC* from the *Autoroute* submenu.

## Autorouting using SPECCTRA

When you select the SPECCTRA autorouter, the complete board is routed. Unlike Layout, which uses grid-based routing, SPECCTRA uses shape-based routing and is a faster routing tool.

To use the SPECCTRA auto router,

1 From the *Auto* menu in Layout, choose *Autoroute* and then select *SPECCTRA*.



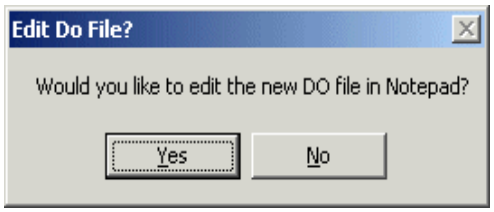

2 In the SPECCTRA interface dialog box, specify the location of the SPECCTRA exe to be used.

In the demo CD, SPECCTRA is located at `<install_dir>/OrCAD/OrCAD_10.0_Demo/tools/specctra/bin`.

3 Specify the name and location of the .DO file to be used for running SPECCTRA.

To create a DO file for the full adder design, click Create.

4 In the message box that appears, click NO.



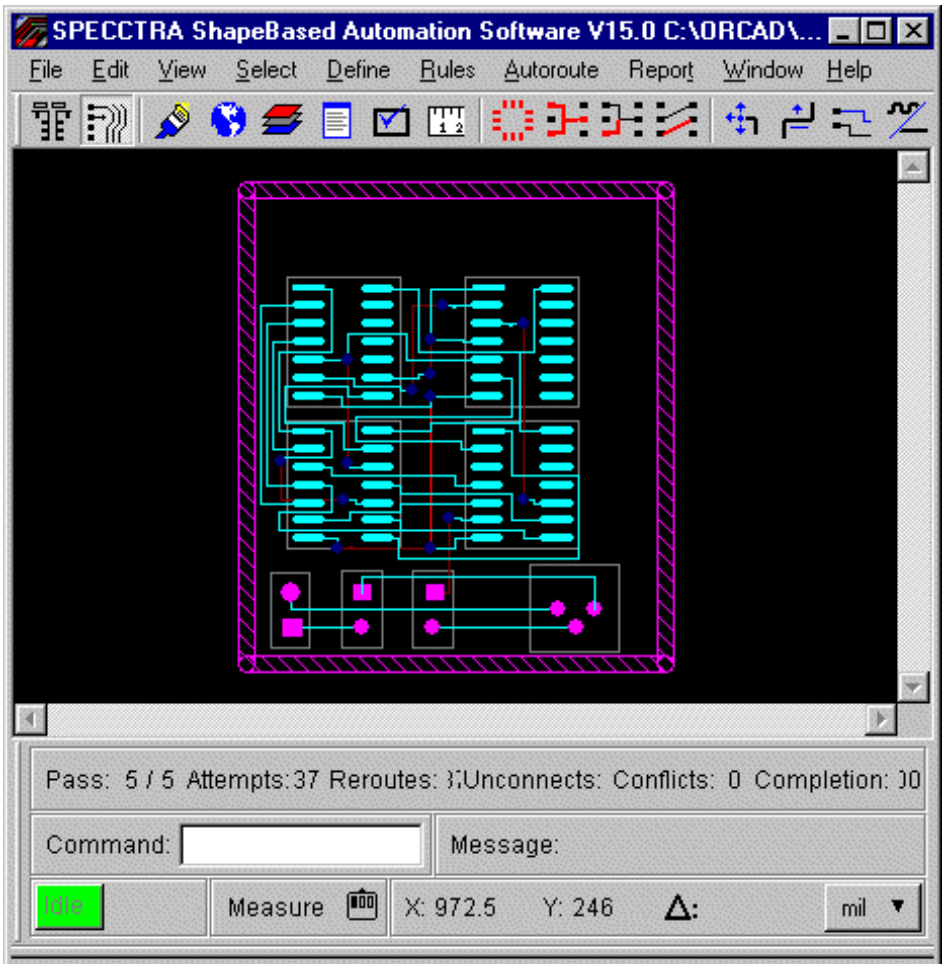

5 The name and the location of the DO file created by OrCAD Layout appears in the text box. By default, a file named `SpecctraWithinLayout.do` is generated.

6 To start Autorouting, click Route.

A message box appears stating that SPECCTRA licenses are not available and the demo version of the tool will be launched.

7 Click OK to start the demo version of SPECCTRA.

8 The autorouting process starts and the board is routed as shown in the figure below:




*Important*

The demo version of SPECCTRA does not allow you to save any files generated in SPECCTRA. Therefore, you can only view the routed board but will not be able to back-annotate the information in OrCAD Layout.

To know more about SPEECTRA, see the SPECCTRA tutorial available with the demo CD. To open the tutorial, from the Start menu, choose *Programs > OrCAD 10.0 Demo > Tutorials > SPECCTRA > SPECCTRA Tutorial*.

*Tip*

After you have routed your design, you should again run DRC to confirm that there are no design rules violation in the design.

# Post-processing

This section introduces some of the tasks that are not a part of the placement and routing process, but are related and can be performed using OrCAD Layout.

To know more about post-processing, see *Chapter 13, Post Processing* in the *OrCAD Layout User's Guide*.

## Renaming components

After you have completed the placement and routing of your PCB board, you can rename the components on the PCB board in a specific order.

1. From the *Options* menu, choose *Components Renaming*.

   The Rename Direction dialog box appears.

2. Select one of the renaming strategies.

   For the full adder design, select *Right, Down*.

3. Click OK.

4. From the *Auto* menu, choose *Rename Components*.

Layout renames the components. The reference designators for the component on the board changes.

**Note:** After renaming of components, Layout displays a message box stating that you must backannotate the changes to Capture before running AutoECO.

*Tip*

If you do not want a component to be renamed, you can do so by selecting the Do Not Rename option in the edit Component dialog box.

## Back annotation

While creating a PCB board, you might make some changes in the layout board (.MAX) file. As a result, the board file and the design file in Capture may be out of sync. To ensure that both these file are in sync, you can backannotate the changes in the PCB board file to the Capture.

When you backannotate, information, such as component location and component names (changed due to renaming) gets added on to the schematic in Capture.

To generate the backannotation file:

1. From the *Auto* menu in Layout, choose *Back Annotate*.
2. A message box indicating the location of FULLADD.SWP file appears. Click OK.

The `.SWP` file generated by Layout after backannotation is read by OrCAD Capture.

To know more about the `.SWP` file, see *OrCAD Capture User's Guide*.

To backannotate the changes to the schematic:

1. Open `FullAdd.opj` in Capture.
2. In the Project Manager window, select `fulladd.dsn`.
3. From the *Tools* menu in Capture, select *Back Annotate*.
4. In the Backannotate dialog box, select the *Process entire design* option button.

5 Select the *Update Occurrences* option button.

**Note:** Ignore the warning stating that this is not the preferred mode of operation.

6 Specify the location of the `.SWP` created by Layout.

7 Click OK.

The schematic is updated with the changes in the board file.

Similarly, if the board file is open in Layout and you make changes in the schematic design, you can ensure that these changes are forwarded to the board during Layout netlist creation.

To do this:

1 In the Project Manager window, select the `fulladd.dsn`.

2 From the *Tools* menu, choose *Create Netlist*.

3 In the Layout tab of the Create Netlist dialog box, select the *Run ECO to Layout* check box.

4 Click OK.

The changes in the schematic design will appear in the board file.

## Cross probing

OrCAD Layout is tightly integrated with OrCAD Capture. As a result, you can use cross-probing to verify information flow between the schematic design and the board design.

Cross probing lets you select an object in he Capture schematic and see the corresponding net highlighted in OrCAD Layout.

To enable cross-probing, you need to enable intertool communication between Capture and Layout. To do this:

1 In the Project Manager window in Capture, select `fulladd.dsn`.

2 From the *Options* menu in Capture, choose *Preferences*.

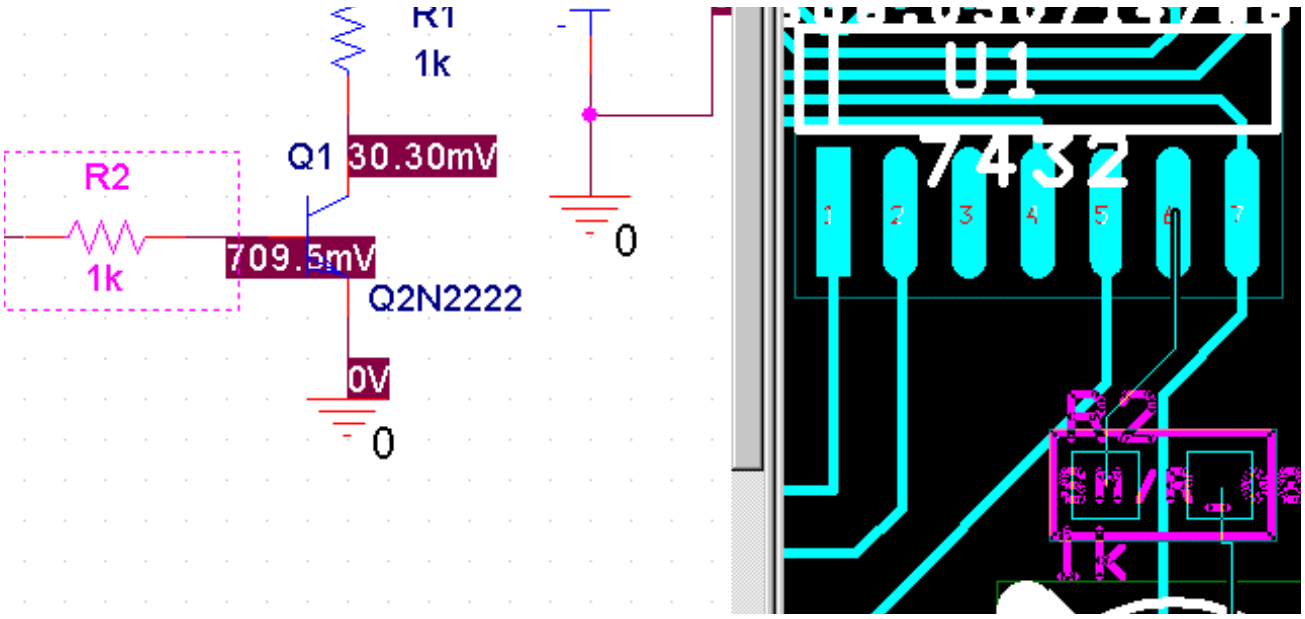
3 Click the Miscellaneous tab.

4 Ensure that the *Enable Intertool Communication* check box is selected in the Intertool Communication section.

5 Click OK.

Before you start cross probing, tile the Capture and Layout windows. Select a component in Layout. OrCAD Capture automatically opens the schematic page containing the component.

For example, if you select R2 in the FULLADD-1.MAX file, resistor R2 will get highlighted in Capture as shown in the figure given below.




# Generating output

The final task in creating a board design is to generate output files. You can create Gerber files, drill files, DXF files, and printer/plotter files.

Before you generate reports and output files, you should clean up the design. To clean up your design:

1 From the *Auto* menu, choose *Cleanup Design*.

The Cleanup Design dialog box appears.

2 In the Cleanup Routing section, click the Select All button.

3 In the Cleanup Database section, select all three check boxes, to ensure that unused padstacks, footprints, and Nets are removed.

4 Click OK.

Message boxes appear indicating the cleanup process being performed. You can now generate the desired output files and reports.

## Output files

Using OrCAD Layout, you can generate various files that can further be used with various third-party tools, such as GerbTool, IntelliCAD, VisualCAD, AutoCAD, and so on.

To generate these output files, complete the following steps:

1 From the *Options* menu, choose *Post Process Settings*.

The Post Process spreadsheet appears.

Post Process

| Plot output File Name | Batch Enabled | Device | Shift | Plot Title |
|---|---|---|---|---|
| *.TOP | Yes | EXTENDED GERBER | No shift | Top Layer |
| *.BOT | Yes | EXTENDED GERBER | No shift | Bottom Layer |
| *.GND | Yes | EXTENDED GERBER | No shift | Ground Layer |
| *.PWR | Yes | EXTENDED GERBER | No shift | Power Layer |
| *.IN1 | No | EXTENDED GERBER | No shift | Inner Layer 1 |
| *.IN2 | No | EXTENDED GERBER | No shift | Inner Layer 2 |
| *.IN3 | No | EXTENDED GERBER | No shift | Inner Layer 3 |

2 Select the Device column.

3 Right-click and select *Properties* from the pop-up menu.

The Post Process Settings dialog box appears.

4 Select the required options.

- To create files to be used with Gerber tools, select Gerber RS-2740 or extended Gerber.
- To create files with mechanical information that is to be used with the CAD tools, select DXF.
- To create HPGL files select Print Manager. To create HPGL file, you must have the HPGL printer installed.

In the Post Process Settings dialog box, select the Extended Gerber check box.

5 Select the Create Drill Files, Overwrite Existing Files, and Enable for Post Processing option buttons.

6 Click OK.

Gerber files are generated.

7 Close the Post Process spreadsheet.

You can also generate output files using the Run Post Processor command.

1 From the *Auto* menu, choose *Run Post Processor*.

2 A message box appears indicating the generated filename. Click OK.

After Layout creates the post processing files, a post processing log file displays.

## Reports

You can create a variety of reports using OrCAD Layout.

To create reports, complete the following steps:

1 From the *Auto* menu, choose *Create Reports*.
The Generate Reports dialog box appears.

2 Select the reports you want generated.
For the full adder design, select the *Comp All (Comps)* check box.

3 Click OK.

## Summary

In this chapter, you were introduced to OrCAD Layout, which is a place-and-route tool provided by OrCAD. You completed the tasks required to take a design from OrCAD, a schematic design tool, to a place and route tool. You were also introduced to SPECCTRA, which is also a tool used to place-and-route the printed circuit boards.

## What's next

This is the last chapter in the OrCAD Flow Tutorial. In the Glossary, you will find the definitions of various terms used in this tutorial.

## Recommended reading

For more information about OrCAD Layout, see *OrCAD Layout User's Guide* and the OrCAD Layout online help. To know about autorouting using Layout, see *OrCAD Layout Autorouter User's Guide*.

To learn about SPECCTRA, see the *SPECCTRA User Guide* and the *SPECCTRA tutorial*. To launch the SPECCTRA tutorial, from the Start menu, choose *Programs > OrCAD 10.0 Demo > Tutorials > SPECCTRA > SPECCTRA Tutorial*.

To know more about OrCAD Unison flow, see *OrCAD Unison Suites Flow Guide*.

# Glossary

| | |
|---|---|
| **AutoECO** | Acronym for automatic engineering change order. AutoECO is a Layout command that enables you to forward annotate a printed circuit board from OrCAD Capture for Windows (or another design capture package) to Layout. |
| **autorouting** | Automatic routing performed by a computer application based on a set of rules called strategies. |
| **Bill of Material** | A bill of materials is a composite list of all the elements you need for your PCB design |
| **bottom-up methodology** | A design methodology in which you first create lowest level design and then create hierarchical blocks for these lowest-level designs. |
| **Complex hierarchy** | A design in which two or more hierarchical blocks (or parts with attached schematic folders) reference the same schematic folder. |
| **cross probing** | When intertool communication is enabled in Capture, selecting objects in Capture causes the corresponding objects to be highlighted in Layout. Also, selecting objects in Layout causes the corresponding objects to be highlighted in Capture. Both applications must be open. |
| **cross reference report** | A cross reference report contains information such as part name, part reference, and the library from which the part was chosen. |

| | |
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| **design rule** | (For OrCAD Layout)<br>A guideline that specifies any of a number of parameters for the printed circuit board. These may include minimum clearance between items that belong to different nets, or connection rules. Also, these rules may include specifications for track width to carry a given current, maximum length for clock lines, termination requirements for signals with fast rise and fall times, and so on. |
| **Design Rules Check (DRC)** | Design Rules Check (DRC) is executed to isolate any unwanted design errors that might exist in the design |
| **design template** | Is used to specify the default characteristics of your project, such as default fonts, page size, title block, and grid references |
| **DO file** | A .DO file is a text file that contains a sequence of autorouter commands. The order of commands in a do file is very important because the autorouter executes each command in sequence. |
| **flat design** | A schematic design that has no hierarchical blocks or port and has no parts with attached schematic folders. A flat design can have multiple schematic pages such that the output lines of one schematic page connect laterally to input lines of another schematic page using off-page connectors. Flat designs are practical for small designs with few schematic pages. |
| **Hierarchical design** | A design in which schematic folders are interconnected vertically with hierarchical blocks. At least one schematic folder, the root schematic folder, contains symbols representing other schematic folders. |
| **multi-run analysis** | Result in a series of DC sweep, AC sweep, or transient analysis depending on the basic analysis that you enabled. |
| **ratsnest** | Unrouted connection between two pins on a PCB board |
| **Simple hierarchy** | A design in which there is a one-to-one correspondence between hierarchical block (or parts with attached schematic folders) and the schematic pages they |

| | |
|---|---|
| | reference. Each hierarchical block (or part with attached schematic folder) represents a unique schematic page. |
| **surface mount** | A component mounting technology in which holes are not required. |
| **Technology template** | A file that contains a board outline and the appropriate design rules, drawing formats, dimensions for spacing and grids, preplaced components, and tooling holes for a specific type of board. |
| **Top-down methodology** | A design methodology in which you first create top-level design using the hierarchical blocks and then create schematic designs for the hierarchical blocks. |
| **track** | Routed connection between two pins on a PCB board |

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